Cerium oxide nanocrystals for nonvolatile memory applications
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High-pressure deuterium annealing for improving the reliability characteristics of silicon–oxide–nitride–oxide–silicon nonvolatile memory devices
In recent years, cerium dioxide (CeO₂), which has been extensively researched on as the buffer layer for YBa₂Cu₃O₇₋ₓ (YBCO) on sapphire, an electrolyte material of solid oxide fuel cells, buried insulator for silicon-on-insulator, HfO₂ ceramics, is used for the scaling limitations of the conventional flash memories for future nonvolatile, high density, and low power memory devices. Recently, high-κ dielectric NCS on the SiO₂ tunneling layer for silicon-oxide-nitride-oxide-silicon (SONOS)-type memories have been proposed. Lin et al. have reported a method of cosputtering Hf and Si in oxygen followed with high-temperature annealing to form the high-κ NCS for SONOS-type memory devices. However, the HfO₂ nanocrystal memory exhibits saturation windows in channel-hot-electron (CHE) program mode. You et al. have proposed the sol-gel spin-coating method to form the high-κ NCS. This method may increase thickness of tunnel oxide and results in high operation voltage.

In this study, the CeO₂ NCS were produced by a thermal annealing in different ambients. SONOS-type memories were fabricated and the electrical properties were investigated. The CeO₂ NC memory devices have shown good electrical properties in terms of large memory window (> 2 V) at P/E speed of 10/10 μs and a retention time up to 10⁴ s with only 10% charge loss. Our results suggest that the CeO₂ NC formation technique is simple and reliable, which shows a good potential for the application of the future fast nonvolatile memories.

P-type Si (100) substrates with a resistivity of 5–10 Ω cm were used. A thin CeO₂ layer was deposited on SiO₂ tunneling layer by an electron-beam evaporator at 10⁻⁶ Torr. The samples subsequently underwent rapid-thermal annealing (RTA) at 900 °C for 1 min in either O₂ or N₂ ambient to form self-assemble CeO₂ NCs. Afterward, all samples were deposited with a 24-nm-thick blocking oxide layer by using a low-pressure tetraethoxysilane system at 700 °C. A 200-nm-thick polycrystalline silicon (poly-Si) gate was deposited and patterned. The poly-Si gate and source/drain regions were implanted with arsenic (5 × 10¹⁵/cm², 20 keV), and the subsequent dopant activation annealing was performed at 950 °C for 15 s. Finally, the CeO₂ NC memory devices were completed after the substrate etching and metallization. The electrical properties of such devices were measured using HP 4156B semiconductor parameter analyzer and HP 41501A pulse generator.

The cross-sectional transmission electron microscopy (TEM) images of the CeO₂ NCs embedded in the SiO₂ dielectric matrix for rapid-thermal N₂ (RTN₂) and O₂ (RTO₂) samples are shown in Figs. 1(a) and 1(b), respectively. No obvious difference in microstructure in terms of NC size and distribution are formed between annealed samples. They showed a NC density of (3–7) × 10¹¹/cm². The average NC size was 8–10 nm. Crystallized NCs with obviously visible lattice fringes were evident in the insets. Figure 2 shows the ideal energy band diagrams of the CeO₂ NC memory devices. The charges may be trapped in electron and hole traps in the CeO₂ NCs or by charge confinement in the quantum...
well.\textsuperscript{17} Zhang \textit{et al.}\textsuperscript{20} have reported that the CeO\textsubscript{2} band gap is 3.15 eV and Engström \textit{et al.}\textsuperscript{21} have indicated that the conduction band offset between cerium oxide and silicon is 2.7 eV. The quantum well formed by the conduction band is deeper for CeO\textsubscript{2} NC structure than SONOS structure\textsuperscript{2.7 eV} compared to 1.05 eV\textsuperscript{22}.

The programming speed of the CeO\textsubscript{2} NCs memory devices with RTN\textsubscript{2} and RTO\textsubscript{2} annealing are shown in Fig. 3\textsuperscript{a}. The device is programed by CHE injection. When the program voltage increases to 10 V, the $V_{th}$ shift increases rapidly and a memory window greater than 5 V was achieved within 1 ms. The large memory windows make the multilevel operation possible. The fact the programming speed is independent of annealing condition of the charge trapping centers, indicating that the programming speed is primarily dependent on the tunneling oxide. Figure 3\textsuperscript{b} shows the erasing speeds at different voltages with a fixed $V_{d}$ of 10 V. The device is erased band-to-band hot-hole (BBHH) injection. For the erasing speed operation, the device was programed under $V_{g} = 10$ V, $V_{d} = 9$ V with a duration of 0.1 ms. As observed, an increase in the negative gate bias resulted in a high erasing speed due to a higher electrical field for the BBHH injection. A fully erased state was fulfilled within 1 ms when operating two samples at $V_{g} = -7$ V and $V_{d} = 10$ V. We concluded that using the CHE for programming and the BBHH for erasing has achieved high $P/E$ efficiency in the CeO\textsubscript{2} NC memory devices.

Figure 4 shows the data retention characteristics of the CeO\textsubscript{2} NC memory devices with different RTA treatments and programming states. The RTN\textsubscript{2} sample showed a smaller amount of charge loss at room temperature for a retention times up to $10^{4}$ s than the RTO\textsubscript{2} sample. It is conjectured that the bulk traps of RTN\textsubscript{2} sample are deeper than RTO\textsubscript{2} sample so that the charge loss of RTN\textsubscript{2} sample is less than RTO\textsubscript{2} sample. This phenomenon can be ascribed to the fact that sufficiently deep trap energy levels exist in the CeO\textsubscript{2} NCs. At high temperature (85 °C), RTN\textsubscript{2} sample increased charge loss rapidly after $10^{3}$ s. The result is because the charge loss of RTN\textsubscript{2} sample comes from the charge in the bulk traps. The electrons can be either trapped in these bulk defects or stay in the conduction band of the CeO\textsubscript{2} NCs and/or in the interface states between the CeO\textsubscript{2} NCs and SiO\textsubscript{2}.\textsuperscript{17,22}

We have demonstrated higher $P/E$ speed of 10/10 $\mu$s with CeO\textsubscript{2} NC memory devices. The RTN CeO\textsubscript{2} NC trapping layers have a larger charge storage capacity and a longer retention time up to $10^{4}$ s with only 10% charge loss than the RTO sample due to deeper trap center. It is concluded that CeO\textsubscript{2} NCs can be used as discrete charge trapping sites for the SONOS-type memories.

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