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Effects of independent double-gated configuration on polycrystalline-Si nonvolatile memory devices

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A polycrystalline-Si thin-film transistor configured with independent double-gated structure and ultrathin channel film is proposed for use as a Si-oxide-nitride-oxide-Si memory device. Taking advantage of additional control gate bias offered by the independent double-gated scheme in addition to the driving gate, this work demonstrated that the reading window and programming efficiency can be improved by applying a proper control gate bias. It is also found that the relationship between programming/erasing speed and control gate bias is strongly related to channel film thickness. Our results indicate that the independent double-gated device possesses promising potential for future nonvolatile memory applications. © 2009 American Institute of Physics. doi:10.1063/1.3238362

Aggressive scaling of conventional floating-gate (FG) type memory device has encountered quite a few issues that must be seriously dealt with, including narrow FG-FG space to contain control gate, FG-FG interference coupling, read or program noise, and severe short channel effects. To address those issues, charge-trapping type nonvolatile memory (NVM) devices, with nitride read-only memory2 and Si-oxide-nitride-oxide-Si (SONOS) (Ref. 3) being the mainstream, have recently emerged as new promising candidates for continuing the miniaturization trend, along with other innovative NVM concepts, including ferroelectric and magnetoresistive memories,4 phase-change memory,5 and unified random access memory6 that has claimed to have both volatile and nonvolatile functionalities. Among those devices, SONOS, with a plethora of variations such as bandgap engineered SONOS,7 Ta-AlO-nitride-oxide-Si,8 etc., has shown its high performance and promising potential for future flash memory applications.

With more efforts on improving gate controllability over channel, polycrystalline-Si thin-film transistor (poly-Si TFT) is now conceived as an ideal structure for meeting NVM requirements.9,10 The use of an ultrathin body has been shown to dramatically improve the subthreshold swing of the TFT,9 thus enabling high programming/erasing efficiency as well as low voltage operation.11 Recently we had proposed several simple nanowire (NW) TFT preparation methods without the need of expensive lithographic tools.12,13 In this paper, we extended the results of a previous work14 and investigated the impacts of independent double-gated (IDG) configuration and the channel film thickness on the performance of TFT SONOS devices.

Detailed device fabrication process can be found in Ref. 14. In this work, the first gate dielectric, which had been an oxide previously, was replaced by an oxide/nitride/oxide (ONO) stack consisting of 5 nm tunneling oxide, 7 nm nitride, and 7 nm blocking oxide. It should be noted that the originally designed blocking oxide thickness was 10 nm; however, due to technical problems of the furnace system in the fabrication laboratory, the resulting thickness was only 7 nm. Gate dielectric of the second gate is a 15 nm oxide.

FIG. 1. (Color online) (a) Schematic structure and (b) TEM image of a fabricated device.

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Schematic device structure and cross-sectional transmission electron microscopic (TEM) image of the fabricated device are shown in Figs. 1(a) and 1(b), respectively. In Fig. 1(b), the channel thickness (or the width of the poly-Si between the two gate dielectrics) is 11 nm. The device is programmed and erased by Fowler–Nordheim tunneling. Depending on the choice of driving gate, different operational modes are feasible. Demonstrating the merit of the IDG scheme, solid lines in Fig. 2(a) show the transfer curves driven by the first gate with various applied second gate bias ($V_{SG-2}$) ranging from −2 to 2 V. In other words, the second gate serves as the control gate (CG) to adjust the threshold voltage ($V_{th}$) of the transfer curves driven by the first gate. $V_{th}$ is defined as the gate voltage at which the drain current is equal to 10 nA × W/L at $V_D = 0.5$ V. This mode is denoted as the SG-1 mode. It is evident that $V_{th}$ is efficiently adjusted by different $V_{SG-2}$, an effect owing to the high sensitivity of the potential of ultrathin channel layer to both gates. Even after the device is programmed by $V_{SG-1} = 15$ V and $V_{SG-2} = 0$ V for 1 ms while the source and drain are grounded, the $V_{SG-2}$ induced $V_{th}$ modulation is still apparent, shown as dashed lines in Fig. 2(a). Similar characterization for the SG-2 mode with the first and second gates acting as the control and driving gate, respectively, is given in Fig. 2(b). Their respective $V_{th}$ window ($\Delta V_{th}$), defined as the difference of $V_{th}$ between programmed and fresh states for the two operation modes, is displayed in Fig. 2(c).

The results show that under SG-1 mode, $\Delta V_{th}$ is not highly related to the $V_{SG-2}$. As for the SG-2 mode, Fig. 2(c) demonstrates that $\Delta V_{th}$ depends on the $V_{SG-1}$ to a larger extent. As explained in Ref. 14, since the second gate provides better electrostatic control over channel than the first gate, an effect inherent in this structure, the second gate is able to adjust $V_{th}$ in a much faster rate. Moreover, the $V_{th}$ of programmed states in Fig. 2(b) shows little dependence on the CG bias, which leads to the $\Delta V_{th}$ enlargement with increased CG bias. This $\Delta V_{th}$ discrepancy between two modes is caused by the location of storage charge relative to the driving gate. If the CG is the one with ONO stack, e.g., the first gate, then the trapped electrons in the nitride layer provide screening from the electric field penetration of the CG. Thus, the CG bias has weak influence on the channel potential and $V_{th}$ is independent of the CG bias in the programmed state. From another perspective, for a sufficiently positive CG bias, inversion would first occur at the channel surface near the

![FIG. 2.](image1) Transfer characteristics for fresh and programmed states (a) under SG-1 mode with varying second gate bias and (b) under SG-2 mode with varying first gate bias. (c) Extracted $V_{th}$ window as a function of CG bias for SG-1 and SG-2 modes.

![FIG. 3.](image2) Programming characteristics under the condition of fixed $V_{SG-1} = 15$ V and varying $V_{SG-2}$ for a device with NW thickness of (a) 11 and (b) 50 nm.
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