A Three-Parameters-Only MOSFET Subthreshold Current CAD Model Considering Back-Gate Bias and Process Variation

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Abstract—In this paper we introduce a new subthreshold conduction CAD model for simulation of VLSI subthreshold CMOS analog circuits and systems. This model explicitly formulates the back-gate bias effect and preserves the original advantages of the existing four-parameter model while reducing the fitting parameter number down to three. A transparent relationship between the fitting parameters and the process parameters has been derived, and its correlation with a recently widely used CAD model as well as with a well-known two-parameter model has been established. Our extensive measurement work on n-channel MOSFET's has highlighted the potential of the model in handling the variations in the subthreshold $I-V$ characteristics at different back-gate biases arising from process variations. The mismatch analysis has further been successfully performed with emphasis on the reverse back-gate bias effect. In summary, the proposed model can serve as a promising alternative in the area of VLSI subthreshold CMOS analog circuit simulation.

Index Terms—Back-gate bias, CAD model, CMOS analog circuits, mismatch, subthreshold, process variation.

I. INTRODUCTION

SUBTHRESHOLD operation of a MOSFET has long been utilized for implementation of the very low power, low voltage digital and analog integrated circuits [1], [2]. Recently, a large variety of very large scale integration (VLSI) analog computation systems, realized by a large number of MOSFET’s each operating in the subthreshold region, have been reported [3]–[6]. To greatly reduce simulation cost and time in such large systems especially when performing the mismatch analysis, a simple transistor CAD model with considerable accuracy is of increasing importance [4]. At least three essential features are demanded for the candidate model [4]: 1) the number of the fitting parameters must be as small as possible; 2) the process of parameter extraction must be easy and straightforward; and 3) the back-gate bias effect must be explicitly formulated. It is well recognized that the mismatch analysis plays a crucial role in ensuring successful implementation of the circuit design specially in subthreshold [2], [4], [7], [8]. Thus, the candidate model itself has to be capable of properly reflecting the variations in the subthreshold $I-V$ characteristics due to process perturbations [4]. Many subthreshold conduction models have been published in the open literature; however, as evaluated in detail by Pavasovic [4], these models failed to meet one or more of the above features (refer to [4, Ch. 2]). To overcome this circumstance, Pavasovic [4] has alternatively proposed, without any derivation, an empirically based four-parameter subthreshold current model along with successful demonstration of the abilities in reproducing the back-gate bias effect and in performing the mismatch analysis.

This paper significantly advances the work of [4] in terms of a new subthreshold current CAD model with reduced parameter number, while preserving the original advantages: back-gate bias effect explicitly formulated, and easy and straightforward extraction of the parameters. A transparent relationship between the fitting parameters and the process parameters will be derived, and its correlation with a recently widely used CAD model [6] as well as with a well-known two-parameter model [3] will be addressed. The presented model will be extensively judged experimentally regarding the ability of dealing with the variations in the subthreshold $I-V$ characteristics at different back-gate biases due to process variations. The mismatch analysis will further be performed employing the model.

II. NEW MODEL FORMULATION

A MOSFET subthreshold conduction model suitable for simulation of VLSI subthreshold analog circuits and systems has been published in [4]

$$I_D = I_0 e^{V_{GS}/\kappa U_T} e^{V_{DS}/\eta U_T} (1 - e^{-V_{DS}/U_T})$$

$$\eta = \gamma_0 + \gamma_1 V_{GS}. \tag{1}$$

This model needs four fitting parameters: $I_0$, $\kappa$, $\gamma_0$, and $\gamma_1$. The effect of the back-gate bias $V_{BS}$ was explicitly through the exponential factor associated with $V_{BS}$ as well as through the parameter $\eta$ that is expressed as a function of only the gate-to-source voltage $V_{GS}$. In other words, ignoring the dependence of $\eta$ on $V_{GS}$ [i.e., $\gamma_1 = 0$ in (1)] can seriously deteriorate the ability of reproducing the back-gate bias effect. To our knowledge, however, it is difficult to theoretically derive (1) from any existing subthreshold $I-V$ formulas.

Independently, the following new formulation has been found to be capable of modeling the subthreshold $I-V$ characteristics at different back-gate biases measured from a large
variety of MOSFET’s fabricated by different CMOS processes

\[I_D = I_0 e^{V_{GS}/nU_T} e^{(1-n)/V_{BS}/U_T} (1 - e^{-V_{DS}/U_T})\]

\[n = 1 + \frac{1}{n_0 + n_2 V_{BS}}.\]  

(2)

This new model includes only three fitting parameters: \(I_0\), \(n_0\), and \(n_2\). Apparently, the parameter number needed for the region of interest is reduced by one as compared to (1). The dependence of the subthreshold current on the back-gate bias is explicitly through the exponential factor associated with \(V_{BS}\) as well as through the slope factor \(n\). The parameter extraction process is also easy and straightforward: first \(I_0\) is extracted at \(V_{BS} = 0\), and then \(n_0\) and \(n_2\) are simultaneously obtained using least-square fitting to the other \(I-V\) curves with nonzero \(V_{BS}\). Note that the slope factor associated with \(V_{GS}\) in both models has different meanings: the quantity \(n\) in (2) is a function of \(V_{BS}\), while that (i.e., \(n\)) in (1) is taken to be constant.

A. Relationship Derivation

A transparent relationship between the fitting parameters and the process parameters can be easily derived from one existing subthreshold current expression under certain conditions [9]:

\[I_D = I_X e^{(V_{GS} - V_X)/nU_T} \left(1 - e^{-V_{DS}/U_T}\right)\]  

(3)

where

\[V_X = V_{FB} + 1.5\phi_f + \gamma \sqrt{1.5\phi_f - V_{BS}},\]

\[I_X = \beta e^{\frac{\gamma}{2\sqrt{1.5\phi_f - V_{BS}}} - e^{-\delta \phi_f / U_T}},\]

\[n = 1 + \frac{\gamma}{2\sqrt{1.5\phi_f - V_{BS}}}, \quad \gamma = \frac{\sqrt{2e/\varepsilon_{si}N_A}}{C_{ox}},\]

\[\phi_f = U_T \ln(N_A/n_i).\]

In (3), \(V_{FB}\) is the flat-band voltage; \(\gamma\) is the body effect coefficient; \(\phi_f\) is the quasi-Fermi level \(N_A\) is the channel doping concentration; \(\mu\) is the carrier mobility; \(C_{ox}\) is the gate oxide capacitance per unit area; \(W/L\) is the channel width to length ratio; \(n_i\) is the intrinsic concentration; \(\varepsilon_{si}\) is the silicon permittivity; and \(U_T = kT/q\). Assuming a small \(V_{BS}\), we have

\[\sqrt{1.5\phi_f - V_{BS}} \approx \sqrt{1.5\phi_f} - \frac{V_{BS}}{\sqrt{6}\phi_f}.\]

(4)

Substituting (4) into (3), we can express \(I_0\) and \(n\) compactly

\[I_0 \approx \beta U_T^2 \frac{\gamma}{2\sqrt{1.5\phi_f}} e^{-\delta \phi_f / U_T} e^{-V_{FB} + 1.5\phi_f + \gamma \sqrt{1.5\phi_f} - U_T}/(1 + \gamma/2\sqrt{1.5\phi_f})U_T,\]

\[n \approx 1 + \frac{1}{\gamma} \frac{2\sqrt{1.5\phi_f - V_{BS}} \gamma}{\sqrt{6} \phi_f}.\]

(5)

(6)

Apparent in (2), \(n_0 = 2\sqrt{1.5\phi_f/\gamma}\) and \(n_1 = -2/(\sqrt{6}\phi_f)\). Thus, the three fitting parameters \(I_0, n_0\), and \(n_1\) each are transparently related to the process parameters. From (5) we can observe that the parameter \(I_0\) is essentially independent of, or is a weak function of, the biases, and in practice, can be reasonably regarded as a constant in (2). Equations (5) and (6) can also provide a physical basis for the ability of handling the effect of process variation as explained later. Although theoretically the assumption of \(1.5\phi_f > V_{BS}\) for (4) might limit the range of validity, our extensive experiment strongly points out that the model is applicable in a wide \(V_{BS}\) range as long as the parameters \(n_0\) and \(n_2\) are simultaneously extracted over the same range. In fact, we have found that the conventional method of extracting \(I_0\) and \(n_0\) simultaneously at \(V_{BS} = 0\) can lead to a worse reproduction of the back-gate bias effect.

B. Correlation with Other Models

Now we demonstrate the work of relating (2) to the model cited in [3] with respect to the slope factor \(n\). The latter model is indeed the same as (2) with two fitting parameters \(I_0\) and \(n\). Referring to [3, App. B], the depletion capacitance per unit area \(C_{dep}\) and the oxide capacitance per unit area \(C_{ox}\) both constitute the single parameter \(n\):

\[n = 1 + \frac{C_{dep}}{C_{ox}} = 1 + \frac{1}{2\sqrt{\Delta\phi} / V_{BS}}.\]

(7)

where \(\Delta\phi < \Delta\phi_f < 2\Delta\phi_f\) to ensure subthreshold action. Apparently, if \(\Delta\phi = 1.5\phi_f\) for mid-point consideration and under (4), (7) readily reduces to (6). From (7), another parameterization would be written for the slope factor \(n\) in such a way to account for the weighted average between \(C_{dep}\) and \(C_{ox}\):

\[n = 1 + \frac{1}{n_0 + n_2 \sqrt{V_{BS}}}.\]

(8)

Experimental judgment of (8) will be given later. Note that in the text of [3], the slope factor \(n\) was taken as a constant independent of the \(V_{BS}\), i.e., in [3] (2) with \(n_1 = 0\) was employed throughout and also applied for derivation of the macromodel for several subthreshold circuit blocks. However, ignoring the third parameter \(n_2\) can give rise to an unacceptable loss in precision.

Recently, a MOSFET CAD model as cited in [6] has been widely utilized for circuit simulation. Its subthreshold conduction expression reads

\[I_D = 2n/\beta U_T^2 e^{(V_{GS} - V_{th0} - nV_{BS})/nU_T},\]

(9)

where \(V_{th0}\) is the threshold voltage at zero \(V_{BS}\) and \(n < 2\). Apparently, (9) can be made equal to (2) through the following transformation:

\[I_0 = 2n/\beta U_T^2 e^{(V_{th0} - nU_T)},\]

(10)

Indeed, neglecting the fact that the slope factor \(n\) is dependent on the \(V_{BS}\) will produce an unacceptable loss in precision. Equation (10) can provide a theoretical basis concerning the ability of the model in handling the process variation dependencies as demonstrated later. A further analysis by combining (10) and (5) yields

\[V_{th0} = V_{FB} + 2\phi_f + \gamma \sqrt{2\phi_f + m'U_T} \left(n \ln \left(\frac{2n}{n-1}\right) + \frac{0.5\phi_f (n-1)}{U_T} - \gamma \sqrt{2\phi_f + 1.5\phi_f}\right).\]

(11)
Tsividis [9] pointed out the key role of the above term $m'U_T$ in properly defining the threshold voltage. For the first time, (11) expresses this term mathematically. In our work, the $m'U_T$ value based on (11) has been calculated to be around 80 mV. The other features of the above equations such as (6) and (10) are reported in next section.

III. BACK-GATE BIAS EFFECT

A. Experimental Judgment

The proposed new model has been extensively examined by comparing the subthreshold $I$--$V$ characteristics measured from n- and p-channel MOS transistors having different gate widths of 2 to 20 $\mu$m, different gate lengths of 2 to 20 $\mu$m, and four different gate oxide thicknesses of 106, 146, 185, and 227 Å. These large dimensions are the typical values encountered in the present analog circuit design. The measurement setup contained the Keithley 236/238 $I$--$V$ characterization system and a Faraday box for shielding the test wafer, all performed in an air-conditioned room with the temperature fixed at 300 K. These experimental $I$--$V$ characteristics have all been successfully reproduced by the new model over a wide $V_{BS}$ range. Fig. 1 demonstrates one such result for two different gate width to length ratios. Note that in Fig. 1 the subthreshold
current is calculated until the $I_D$ approaches $\beta \mu_p^2$ [2]. Here $\beta \mu_p^2$ as extracted in the above-threshold region are $7.33 \times 10^{-8}$ A and $3 \times 10^{-7}$ A for 20 $\mu$m/20 $\mu$m and 20 $\mu$m/5 $\mu$m n-channel devices, respectively. From Fig. 1, the calculation results from each model seem to match the experimental curves over a wide current range of at least five decades for $V_{BS}$ ranging from 0 to about $-1.8$ V. A clear understanding can be obtained by drawing a plot of the modeling error versus the $V_{BS}$. The modeling error $\varepsilon$ for a given $V_{BS}$ is defined as

$$\varepsilon = \sqrt{\frac{\sum_{i=1}^{M} \left( \frac{I_{\exp} - I_{\text{model}}}{I_{\exp}} \right)^2}{M}}, \quad 1 \times 10^{-12} A < I_{\exp} < 3 \times 10^{-8} A \quad (12)$$

where $I_{\exp}$ represents the measured current, $I_{\text{model}}$ represents the calculation current, and $M$ is the number of data points. The modeling error plot corresponding to Fig. 1 is shown in Fig. 2. From Fig. 2 we can observe that the precision of our model is comparable with the Pavasovic's one over a wide bias range. In Fig. 2, we show the case of making $n_1 = 0$ in (2), which exhibits a rapid increase in error taking place at a relatively small $V_{BS}$. Also plotted in Fig. 2 are the calculated results from (8). Obviously, another parameterization of the slope factor $n$ in terms of $\sqrt{V_{BS}}$ dependence produces a larger deviation from experimental data over the same $V_{BS}$ range. Thus, the first parameterization (2) is favored throughout the work.

### B. Extension to Transition and Above-Threshold Regimes

As described above, the ability of our model in reproducing the back-gate bias effect has been identified experimentally. This is valid as long as the drain current of each MOSFET in the circuits is less than (after the circuit design phase), or is conditionally forced to below (during the circuit design phase), the value of $\beta \mu_p^2$ [2], which ensures the subthreshold operation. To release this limit, one must extend the model to the transition and above-threshold regimes.

In the subthreshold regime, the drain current is dominated by carrier diffusion through the surface depletion region beneath the gate; however, as the $V_{GS}$ is increased above the threshold voltage, the drift component along the inverted surface dominates. The transition regime between the two is a combination of diffusion and drift components in a complicated manner. Different mathematical techniques for empirically smoothing the $I-V$ characteristics of the transition region have been published in the literature [6], [7], [10]–[12]. Here we employ the work of [11] only for demonstration

$$I_D = I_{\text{diff}} \left( e^{\frac{I_{\text{drift}}}{I_{\text{drift}}}} + \frac{I_{\text{drift}}}{I_{\text{drift}}} \right) \quad (13)$$

where $I_{\text{diff}}$ and $I_{\text{drift}}$ represent the diffusion and drift components, respectively; and $I_{\text{drift}} = \zeta \beta \mu_p^2$ with $\zeta$ as an adjusting parameter. From (13) we have $I_D \cong I_{\text{diff}}$ for $I_{\text{drift}} \ll I_{\text{drift}}$, and $I_{\text{drift}} \ll I_{\text{drift}}$, while for $I_{\text{drift}} \gg I_{\text{drift}}$, we have $I_D \cong I_{\text{drift}}$. Therefore, (13) can appropriately describe the $I-V$ characteristics covering the subthreshold, transition, and above-threshold regimes. In this work $I_{\text{diff}}$ is represented by (2) and, due to long channel devices utilized, the following classical equations are reasonably utilized to calculate the component $I_{\text{drift}}$:

$$I_{\text{drift}} = \begin{cases} \left[ \beta (V_{DS} - V_{th}) - \frac{1}{2} V_{DBS} \right], & V_{DS} < V_{GS} \leq V_{th} \text{ and } V_{GS} \geq V_{th} \\ \frac{\beta}{2} (V_{DS} - V_{th})^2, & V_{DS} \geq V_{GS} \geq V_{th} \\ V_{th} = V_{FB} + 2 \phi_f + \gamma \sqrt{2 \phi_f - V_{BS}}, \end{cases} \quad (14)$$

Here, to facilitate the analysis, the threshold voltage $V_{th}$ adopts the usual form. The procedure of reproducing the total $I-V$ curves is described based on Fig. 3: 1) the $\beta$, $V_{FB}$, $\gamma$, and $\phi_f$ in (14) for $I_{\text{drift}}$ are extracted in above-threshold...
Fig. 3. (a) The measured and calculated $I-V$ transfer characteristics along with the modeling error and (b) the measured and calculated transconductance versus gate-to-source voltage along with the modeling error, all corresponding to Fig. 1(b). Both error plots are calculated using (12) but with $1 \times 10^{-12}$ A $< I_{\text{min}} < 1 \times 10^{-12}$ A. The parameter $R_{\text{min}}$ is adjusted to be $3.5 \beta \mu A$ ($= 25.6 \times 10^{-12}$ A) such as to match closely with experimental curves. $V_{FSS} = -0.165$ V, $\phi_f = 0.225$ V, and $\gamma = 0.532 \sqrt{V}$.

and are given in the caption of Fig. 3; 2) the $I_D$, $n_0$, and $n_1$ values as given in the caption of Fig. 1(b) are used for $I_{\text{eff}}$, and 3) finally the $\zeta$ in (13) is adjusted for best fitting. In such a way, $\zeta \beta \mu A = 3.5 \beta \mu A$ is extracted in Fig. 3. This value is close to the associated parameter $2n_1 \beta \mu A$ in [6] if $n_1 = 1.5$ is typically considered. The calculated and measured $I-V$ curves over the whole region of operation with $V_{BS}$ as a parameter are illustrated in Fig. 3, where the measured and calculated transconductance $g_m(= \partial I_D/\partial V_{GS})$ versus gate-to-source voltage with $V_{BS}$ as a parameter is together plotted. Also plotted in Fig. 3 are the modeling errors based on (12) but with a wider current range. From Fig. 3 we can observe that the calculated results have a maximum error of 23% over a wide bias range. In the analog circuit simulation it is needed to maintain the continuity of the transconductance $g_m$ in the whole operating region. As shown in Fig. 3, no discontinuity of $g_m$ is produced in the transition region between subthreshold and above-threshold. This is essentially due to the mathematical smoothing action as widely employed in the field [6], [7], [10]–[12].

IV. PROCESS VARIATION

The ability of the model in properly handling the variations in the subthreshold $I-V$ characteristics due to process vari-
Fig. 4. The scattering plot of (a) $\ln(I_0)$ versus $V_{th}/n$ and (b) $\ln(I_0)$ versus $V_{th}$ for three different gate width to length ratios at $V_{BS} = 0$ V. The straight lines obtained by least square fit to the data points are also shown. $R$ represents the correlation coefficient.

The scattering plot has been extensively judged experimentally. Here we present such results from the $n^+$-gate n-channel LDD MOSFET devices having three different gate width to length ratios of 20 $\mu$m/20 $\mu$m, 20 $\mu$m/5 $\mu$m, and 20 $\mu$m/2.4 $\mu$m, all formed on chip by a 0.6-$\mu$m twin-well polysilicon CMOS process. The starting material was p-type 100-oriented Si wafers with resistivity of 8–12 $\Omega$-cm. Boron ($6 \times 10^{12}$ cm$^{-2}$, 60 KeV) was implanted to form the p-well region. BF$_2$ ($2.6 \times 10^{12}$ cm$^{-2}$, 70 KeV) was used as the threshold voltage implant. The gate oxide was grown in dry O$_2$ at 920°C to a thickness of 146 Å. After $n^+$ gate polysilicon was formed, phosphorus ($2.0 \times 10^{13}$ cm$^{-2}$, 45° angle rotating, 60 KeV) and arsenic ($3.0 \times 10^{15}$ cm$^{-2}$, 80 KeV) were implanted to form the low-doped and highly doped source/drain regions, respectively.

Each of the devices has been characterized across the wafer, and the variations in the $I$–$V$ characteristics due to process variations have been recorded for subsequent analysis. The measurement setup and environment have been described above. The variations in the subthreshold $I$–$V$ characteristics can be appropriately represented by the variations of the extracted $n_0$, $n_1$, and $I_0$ in (2). The corresponding variations in the above-threshold $I$–$V$ characteristics have also been measured, which can be appropriately represented by the variations in the threshold voltage $V_{th}$. This implies that the
Fig. 5. The scattering plot of $n$ versus $V_{th}$ at (a) $V_{BS} = -1\,\text{V}$ and (b) $V_{BS} = -2\,\text{V}$. The straight line obtained by least-square fit to the data points is also shown. $R$ represents the correlation coefficient.

variations in $n_0$, $n_1$, and $I_0$ due to process variations can be reflected by the variations in $V_{th}$ and thus can be traced by constructing the correlations between the two in advance. The reason and evidence are given in detail later.

First, the case of zero back-gate bias is addressed. The scattering plot of the measured $\ln(I_0)$ versus $V_{th}$ at $V_{BS} = 0\,\text{V}$ for three different gate-width-to-length ratios is shown in Fig. 4(a). Also shown in Fig. 4(a) are three straight lines each calculated by the regression equation. This regression equation offers $R$ values of 0.9892, 0.9798, and 0.9585 for the devices with three different gate-width-to-length ratios of 20 $\mu\text{m}$/20 $\mu\text{m}$, 20 $\mu\text{m}$/5 $\mu\text{m}$, and 20 $\mu\text{m}$/2.4 $\mu\text{m}$, respectively. Here the correlation coefficient $R$ associated with the regression equation has been calculated according to [13]

$$R = \frac{\sum_{i=1}^{N} (X_i - \bar{X})(Y_i - \bar{Y})}{\sqrt{\sum_{i=1}^{N} (X_i - \bar{X})^2 \sum_{i=1}^{N} (Y_i - \bar{Y})^2}} \quad (15)$$

where $N$ denotes the sample number, $X$ and $Y$ are the pair values of the two parameters, and $\bar{X}$ and $\bar{Y}$ are the corresponding mean values. The sample number $N$ is ten for each gate width to length ratio. Note that even with such a
small sample number, the high $R$ values in Fig. 4(a) really show a strong correlation between $\ln(I_0)$ and $V_{th}/n$. The interpretations responsible are given as follows. From (10), we have

$$\ln(I_0) = \ln(2n\beta U_T^2) - \frac{V_{th0}}{\left(1 + \frac{1}{n_0}\right)U_T}$$

$$n_0 = \frac{2\sqrt{1.567/\gamma}}{\phi_f}$$

which gives a linear relationship between $\ln(I_0)$ and $V_{th}/n$ at $V_{DS} = 0$ V, thus providing the origin of the regression line empirically found above. From (16), one can clearly see that the variation in $n_0$ is due to the variation in the process dependent parameters $\gamma$ and $\phi_f$. Equation (16) also explicitly shows that the negative inverse of the slope of the straight line yields a fundamental physical parameter and can be readily applied to check the validity of (16) in a physical manner. It can be shown from Fig. 4(a) that three straight lines offer the slope values of $-34.36$, $-37.38$, and $-39.60$ 1/V, each in reasonable agreement with the inverse of $-kT/q (= -38.68$ 1/V at 300 K). Further calculation on the intercept $\ln(2n\beta U_T^2)$ gives the values of $-13.2$, $-14.6$, and $-15.3$ for the 20 $\mu$m/2.4 $\mu$m, 20 $\mu$m/5 $\mu$m, and 20 $\mu$m/20 $\mu$m devices, respectively, each being consistent with those empirically obtained in Fig. 4(a). Thus, our subthreshold model is capable of explicitly handling the effect of process variation. On the other hand, if the correlation is made between $\ln(I_0)$ and $V_{th}$ as shown in Fig. 4(b), a relatively small value of $R$ is obtained. This indicates that the threshold voltage $V_{th}$ has a strong correlation with the parameter $n$ in (2), and thus the single parameter in terms of $V_{th}/n$ can compensate for the variations in $n$, as originally proposed by Godfrey [7]. In addition, we have found experimentally such strong relationships between $V_{th}$ and $n$ in (2), all measured at two different nonzero back-gate biases, as demonstrated in Fig. 5. This observation can be satisfactorily interpreted by combining (6) and (14) with the common factor $\gamma$ removed, which yields for a given $V_{BS}$

$$n = a + bV_{th}$$

where $a$ and $b$ are two coefficients including the $V_{BS}$. Therefore, the variation in $n$ in (2) can be calculated directly from the measured variation in threshold voltage, which in turn can yield the parameter $I_0$ value by using (16).

V. MISMATCH ANALYSIS

Here the application of the new model in mismatch analysis is given. First, the back-gate bias dependent $I-V$ characteristics have been measured from the on-chip n-type MOSFET’s having the same gate width to length ratio of 2 $\mu$m/2 $\mu$m with a large sample number of 96, as depicted in Fig. 6 for two different $V_{BS}$. From Fig. 6 one can observe that 1) the drain current in subthreshold has a larger spread than in above-threshold and 2) the back-gate reverse bias produces a larger spread in the drain current especially operated in subthreshold. The latter observation can be clearly understood.
by drawing the histogram of the measured subthreshold drain currents. Fig. 7 shows such histograms for \( V_{GS} = 0.58 \) V at zero back-gate bias as well as for \( V_{GS} = 1.2 \) V at \( V_{BS} = -2.0 \) V. From Fig. 7 we can observe that the measured distribution broadens as \( V_{BS} \) is changed negatively from 0 to \(-2.0\) V, indicating that the back-gate reverse bias as usually encountered in subthreshold CMOS circuits can worsen the mismatch in current. This is in agreement with the recent experiment from the current mirrors [14], [15]. The mean \( m \) and standard deviation \( \sigma \) of the measured distributions are labeled in Fig. 7.

From (2), the standard deviation in \( I_D \) can easily be derived explicitly as a function of the standard deviations in \( I_0, n_0, \) and \( n_1 \) [13]:

\[
\frac{\sigma^2_{I_D}}{I_D} = \left( \frac{\partial \ln(I_D)}{\partial I_0} \right)^2 \sigma^2_{I_0} + \left( \frac{\partial \ln(I_D)}{\partial n_0} \right)^2 \sigma^2_{n_0} + \left( \frac{\partial \ln(I_D)}{\partial n_1} \right)^2 \sigma^2_{n_1} \tag{18}
\]

Now we demonstrate how to reproduce the measured mismatch in Fig. 7 by means of both (2) and (18). First the parameters \( n_0, n_1, \) and \( I_0 \) in (2) have been extracted accordingly for each device with \( V_{BS} \) ranging from 0 to \(-2\) V in steps.
of $-0.2$ V, creating the histograms with a large sample number of 96 as depicted in Fig. 8. From Fig. 8, the mean and standard deviation of the $I_D$, $\theta_{\sigma}$, and $\tau_1$ are obtained. Substituting these values into (2) and (18), the mean and standard deviation of the current $I_D$ are calculated as together labeled in Fig. 7 and are found to coincide with the experimental values. Also plotted in Figs. 7 and 8 are the curves of the Gaussian or normal distribution $f(y)$:

$$f(y) = \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{1}{2} \left( \frac{y - \mu}{\sigma} \right)^2}$$  \hspace{1cm} (19)$$

where $y$ is the dummy variable. The reason for utilization of (19) in our work is that the process variation distribution is usually of Gaussian type [16], [17]. Note that $I_D$, $\theta_{\sigma}$, and $\tau_1$ each include explicitly the process parameters, as clearly depicted in (5) and (6). From Fig. 7 we can observe that the calculated distribution curves are comparable with those established empirically. Reasonable agreements in Fig. 7 thus validate the ability of the new model in properly reflecting the dependencies of the subthreshold current simultaneously on the process variations and back-gate biases.

VI. CONCLUSIONS

A new three-parameters-only subthreshold current CAD model taking into account the effects of back-gate bias and process variation has been introduced. A transparent relationship between the fitting parameters and the process parameters has been derived, and its correlation with other models has been assessed. This model has successfully reproduced a large amount of experimental data from different size devices in a wide back-gate bias range. Application of the model to handle the process variation as well as to perform the mismatch analysis has been demonstrated in detail. The other applications of the model, such as correct establishment of the dependencies of the subthreshold current simultaneously on the process variations and back-gate biases.

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REFERENCES


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