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Low-Temperature Polycrystalline Silicon Thin Film Transistor Nonvolatile Memory Using Ni Nanocrystals as Charge-Trapping Centers Fabricated by Hydrogen Plasma Process

Terry Tai-Jui Wang, Pei-Ling Gao, William Cheng-Yu Ma\textsuperscript{1}, and Cheng-Tzu Kuo\textsuperscript{2,*}

Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu 30050, Taiwan
\textsuperscript{1}Institute of Electronics, National Chiao Tung University, Hsinchu 30050, Taiwan
\textsuperscript{2}Department of Materials Science and Engineering, MingDao University, Changhua 52345, Taiwan

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Processes for fabricating a Ni nanocrystal (NC)-assisted low-temperature polycrystalline silicon thin film transistor (LTPS-TFT) nonvolatile memory device of noble stack below 600°C were successfully developed. The NCs were fabricated in H-plasma atmosphere by heating a nanosized Ni film to realize an appropriate nanoparticle distribution. Results show that NCs with a number density of $\sim5 \times 10^{15} \text{cm}^{-2}$ and a particle diameter of 4 to 12 nm can successfully be fabricated as charge-trapping centers for enhancing the device performance. The results also indicate that the data retentions at the initial time and after 10\,s for a SiO$_2$/Ni-NCs/Si$_3$N$_4$/SiO$_2$ gate under the present stack of devices are about 2.2 and $\sim1.1$ V, respectively.} \textsuperscript{©} 2010 The Japan Society of Applied Physics

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1. Introduction

Recently, the NAND flash has become more popular for mobile electronic products, and the demand for memory density is multiplied every year. Although the NAND flash is aggressively scaled down, it becomes continuously difficult to follow Moore’s law owing to physics limitations. As the device size is aggressively scaled down, it becomes continuously difficult to follow Moore’s law owing to physics limitations. A three-dimensional (3D) multilayer-stack memory was proposed as one of the methods for realizing an ultrahigh-density memory.\textsuperscript{1–4)} Furthermore, a nonvolatile memory is aggressively scaled down, it becomes continuously difficult to follow Moore’s law owing to physics limitations.

2. Experimental Methods

Figure 1 shows the TFT-NVM device structure with the embedded Ni-NCs. The SiO$_2$/Si$_3$N$_4$/Ni-NCs/SiO$_2$ gate stack is shown. Fig. 1. (Color online) Structure of TFT-flash memory with Ni-NCs. The SiO$_2$/Si$_3$N$_4$/Ni-NCs/SiO$_2$ gate stack is shown.

deposition (CVD) system is a popular and favorable process for integration with the formation of low-temperature polycrystalline silicon (poly-Si) TFT devices.

E-mail address: kuoct@mdu.edu.tw
to form a Si$_3$N$_4$/SiO$_2$/poly-Si/SiO$_2$/Si stack by PECVD with SiH$_4$, NH$_3$, and N$_2$O as reaction gases. For NC formation, an approximately 5 nm wetting layer of pure nickel was deposited on the stack by sputtering and then H-plasma treatment. The distribution and morphology of Ni-NCs were manipulated by varying the process parameters. On top of NCs, a 15-nm-thick SiO$_2$ blocking dielectric layer was deposited by PECVD, which was followed by O$_2$ treatment to densify the blocking layer. The TFT stack devices were completed by gate definition with solution etching to form Ni-NC structures in the order from top to bottom are an Al electrode, 20 nm Ni-NCs embedded SiO$_2$, a 3 nm Si$_3$N$_4$ buffer layer, a 7 nm SiO$_2$ tunneling layer, and a poly-Si channel layer. There are six black dots in Fig. 5 that represent Ni-NCs with sizes ranging from 4 to 9 nm.

3. Results and Discussion

Regarding the H-plasma treatment performed to form Ni-NCs, the results show that the dot size and number density of NCs are functions of microwave power (600 to 900 W) and treatment time (1 to 10 min). The dot size and number density result from the competitions among heating ability, etching effect, dot fluidity, and dot agglomeration due to the surface tension effect. Under the present study conditions, the number density of Ni-NCs at 900 W for 3 min (5 \times 10^{11} \text{cm}^{-2}) is about one order greater than that at 750 W for 3 min (3.8 \times 10^{10} \text{cm}^{-2}), as shown by SEM micrographs in (a) and (b), respectively.

Fig. 2. SEM morphologies of the H-plasma-treated Ni-NCs on Si$_3$N$_4$ layer for 3 min treatment time at different microwave powers: (a) 900 and (b) 750 W. The number density of Ni-NCs at 900 W for 3 min is about one order greater than that at 750 W for 3 min, as shown by SEM micrographs in (a) and (b).

Fig. 3. SEM morphologies of H-plasma-treated Ni-NCs for 900 W microwave power at different treatment times: (a) 1, (b) 3, (c) 5, and (d) 10 min. The figure suggests the greatest etching effect, which is the bombardment of NCs out of the surface at the treatment time of 10 min.

Fig. 4. Curves of dot number density and mean diameter of Ni-NCs versus H-plasma treatment time. The highest number density of NCs is observed at the treatment time of approximately 3 min.

The $I_D$-$V_G$ features with various current densities (maximum is 0.58 mA/\mu m$^2$) of the Ni-NC-assisted low-temperature poly-Si thin film transistors (LTPS-TFTs) with gate voltages ranging from 0 to 6 V are depicted in Fig. 6. The features signify that the highest current density in this case is favorable for integrated circuit applications. Figure 7 shows the corresponding four different $I_D$-$V_G$ curves of these devices with or without Ni-NCs and with gate program-erase biases of 12 V for 1 s and $-12$ V for 1 s. The $V_{TH}$ shift of the device with Ni-NCs is about 2.2 V in contrast to $-0.1$ V for the device without NCs. The $V_{TH}$ shift of 2.2 V is sufficiently high to be sensed as either “1” or “0” by the sensing amplifier. In addition, the on/off current ratio can increase up to 5 orders with an on-current of $10^{-5}$ A, and the value of the subthreshold swing (SS) can decrease down to $\sim 0.5$ V/decade, signifying a rapid response of the device and a low leakage current of the poly-Si channel. The significance
of the curves can be understood from the following device functions. When the device is programmed, the electrons are tunneled from the Si substrate through the tunnel oxide layer and trapped in the Ni-NCs. When the device is erased, the holes are tunneled from the Si substrate through the tunnel oxide layer and recombine with the electrons. The function of the top SiO$_2$ control oxide layer is to prevent the injection of the carriers of the gate electrode into the Ni-NCs by Fowler–Nordheim (FN) tunneling, as shown in Figs. 8(a) and 8(b). However, using the asymmetric SiO$_2$/Si$_3$N$_4$ tunneling barrier, electrons or holes can be more easily tunneled than only using SiO$_2$ as the tunneling oxide layer. In other words, these devices require a lower operating voltage or a lower power consumption to pump electrons in and out. It can be concluded that the SiO$_2$/Si$_3$N$_4$/Ni-NCs/SiO$_2$ stack of gate dielectric layers has been demonstrated successfully to manipulate the charging and discharging of electrons in the stack for potential applications in nonvolatile memory devices.

The two curves of retention time versus $V_{TH}$ for TFT-NVMs with Ni-NCs in the device at room temperature are shown in Fig. 9 for two different states. These curves show that the devices with Ni-NCs and the program/erase (P/E) condition of $\pm 12$ V for 1 s can maintain a memory window of $\pm 2$ V for a retention time of $10^4$ s. In general, the leakage current of a TFT is a more critical factor in the reverse bias region, known as the Frenkel–Poole (FP) region, in which the trapped electrons can be more easily tunneled out through defects in the tunnel oxide layer by the FP mechanism. In other words, the application of Ni-NCs in the NVM device can improve electron retention through minimizing FP leakage. This may be due to the fact that electrons can be distributed and stored in many NCs, which are insulated to each other to minimize the possibility of simultaneous leakages from all NCs. In addition, the high work function ($\sim 5.15$ eV) of Ni-NCs yields a deep energy well for storing carriers, enhancing data retention.
4. Conclusions

Processes of fabricating Ni-NCs by hydrogen plasma treatment in a CVD system on a Si₃N₄ layer were successfully developed to obtain optimum process parameters for application in LTPS-TFT NVM devices. Results show that an approximately 5-nm-thick Ni film can be used to fabricate NCs with number densities of up to \( \frac{5}{2} \times 10^{11} \text{cm}^{-2} \) at 900 W for 3 min H-plasma treatment. The corresponding TFT-NVM obtained using Ni-NCs as charge-trapping centers has been successfully demonstrated, indicating the possibility of fabricating a 3D multilayer-stack device below 600 °C for ultrahigh-density nonvolatile memory application. Further improvement of the TFT-NVM can be feasible.

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Fig. 9. Data retention curves of Ni-NC-assisted TFT-NVMs for two different data state conditions. The devices with Ni-NCs and the P/E condition of ±12 V for 1 s can maintain a memory window of ~1.1 V for a retention time of 10⁴ s at room temperature.