A sinusoidal signal and its sampled output values, and the absolute error and variance, are given in Figs. 5 and 6, respectively. They show an estimated maximum absolute error of 89mV and a standard deviation of 50.5mV, i.e., $SNR = 27\text{dB}$.

**Fig. 6 Absolute error and variance**

**Conclusion:** A CMOS snapshot sampling technique suitable for a variety of high speed data acquisition situations, such as the detection of high frequency transients, measurement systems, sonar, radar, or laser systems, etc., has been presented. It uses an optimised inverter chain for sample control and simple track-and-hold-circuits for highest speed and low current consumption. Simulations indicate a data acquisition time of 0.34ns, which represents a reduction of 71.7% compared to that obtainable using CMOS inverters, and a maximum absolute error of 89mV ($SNR = 27\text{dB}$) for a simple 0.8-μm digital CMOS process. The maximum input signal frequency is limited to ~0.5–1 GHz, according to high switch resistance for a sample capacitance of 300fF.

**Acknowledgment:** The authors are grateful to M. Karlsson for valuable discussions. This work is financially supported by the Swedish National Board for Technical Development (NUTEK).

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Electronics Letters Online No: 19970746

H. Träff and J. Wikner (Electronics Systems, Department of EE, Linköping University, S-581 83 Linköping, Sweden)

E-mail: hakant.isy.liu.se

**References**


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**Suppression of boron penetration by using inductive-coupling-nitrogen-plasma in stacked amorphous/polysilicon gate structure**

Wen Luh Yang, Chiou-Jyi Lin, Tien Sheng Chao, Don-Gey Liu and Tan Fu Lei

Indexing terms: MOS integrated circuits, Plasma

A method is introduced for suppressing the penetration of boron for BF$_2$-implanted pMOS devices with a stacked amorphous/poly-Si (SAP) gate structure. It is shown that after inductive-coupling-nitrogen-plasma (ICNP) treatment, boron diffusion through the thin gate oxide is largely suppressed. As shown from the charge-to-breakdown measurements, the ICNP process will improve the quality of pMOS devices, with $Q_{bd}$ three times higher than for the control samples.

**Introduction:** It has been proposed that the surface channel structure with a p'-poly-Si gate implanted by BF$_2$ can be adopted to improve the charge control characteristics of pMOS devices in deep submicrometre CMOS applications [1]. However, it has also been found that the boron atoms tend to penetrate through the gate oxide. Consequently, surface-channel pMOS devices suffer several thermal stability problems, such as shifts in threshold voltage, distorted capacitance-voltage characteristics, and high voltage swing in the subthreshold region. Several techniques to improve this have been proposed which can be categorised into two approaches. First, a nitrogen layer can be introduced, as a diffusion barrier, which is piled up at the layer interfaces between the gate, oxide and substrate. This nitrogen barrier can be established by incorporating N$_2$O during the oxidation process [2]. Nitridising the oxide layer by several kinds of ambient, such as H$_2$ [3–5]. The second approach is to modify the gate layer structure with a stacked structure; boron atoms will easily segregate at each layer interface [6]. In this Letter, a novel low temperature process, termed ICNP treatment, is proposed to introduce nitrogen into the gate/oxide and oxide/Si interface with the advantages of a stacked gate structure. In this study, wafers are immersed in the nitrogen plasma created in an inductive-coupling chamber. Since there is no RF power connected to the substrate in the chamber, no DC bias will be exerted on the device surface. The effect of ion bombardment can be eliminated.

**Experiments:** In this study, MOS capacitors with a p'-poly-Si gate were fabricated on the (100)-oriented n-type substrates. An 8nm thick thermal oxide layer was first grown in an ambient of dry oxygen at 900°C. After this stage, an amorphous silicon (a-Si) film is deposited on the wafers at a temperature of 350°C. The film thickness is designed to range from 10 to 30nm to investigate the suitable a-Si layer thickness in the SAP structure. These samples were then subjected to ICNP treatment with various process times. In this study, both the RF power and the N$_2$ flow rate were kept constant at 150W and 50sccm, respectively. The amount of N$_2$ introduced into the gate layer is expected to be affected only by the process time. A following poly-Si film was deposited at 620°C on the a-Si layer to make the total thickness of the gate layer up to 300nm. All the wafers were thereafter implanted by BF$_2$, with a dosage of 5×10$^10$ cm$^{-2}$ and an energy of 50keV. These samples were annealed under an ambient of dry oxygen at 900°C for 10, 20, and 50min that will drive boron into different depths.

**Fig. 1 Charge-to-breakdown of MOS for various a-Si thicknesses against various ICNP plasma time after annealing at 900°C for 50min**

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boron is less significant, even though the total gate thickness of each sample is the same. Studying the effect of the ICNP process time on the purely poly-Si gate layer, i.e. 'without a-Si' curve in Fig. 1, the \( Q_d \) value will decrease from 3.4 C/cm\(^2\) down to 0.8 C/cm\(^2\) after 20min of ICNP processing. Nevertheless, this negative effect can be diminished in those samples with the stacked gate structure. Studying the relationship between \( Q_d \) and ICNP process time for the samples with an a-Si stacked gate in Fig. 1, the quality of the oxide layer can be improved by using a gate with a thicker a-Si layer. As shown in Fig. 1, the samples with only 10nm thick a-Si will still suffer evident degradation in the oxide layer as the ICNP process continues. Nevertheless, the \( Q_d \) value has been improved, compared to the control sample. According to the results obtained in Fig. 1, the effects of a-Si thickness and the ICNP process duration can be explained as below. By increasing the thickness of the a-Si film, the damaging effect is reduced, hence the sample can then endure a longer processing time. In this study, it is expected that the amount of nitrogen introduced into the gate/oxide interface will be higher by using a long-duration ICNP process to suppress boron diffusion. Therefore, the passivation of nitrogen and the damaging effect of the plasma will compete during the ICNP treatment. When the a-Si layer becomes sufficiently thick, degradation by energetic plasma will be overcome and the nitrogen passivation will then dominate. For the samples with a 20nm a-Si layer, the optimum process time is 10min. The best \( Q_d \) we obtained here was 15 C/cm\(^2\), which is three times higher than that of the control sample with a pure poly-Si gate and without ICNP treatment.

Fig. 2 shows the relationship between the flat-band voltage and the ICNP process time. In general, the ICNP treatment will reduce the flat-band voltage for each sample. This fact means that ICNP can effectively suppress the effect of boron penetration. However, seeing the curve for the pure poly-Si gated samples, this passivation effect will fade out as the ICNP process time increases up to 20min. This degradation may also be attributed to the damaging effect of the plasma, as mentioned above. As seen in Fig. 2, it is consistent with the results found in Fig. 1 that the stacked structure can be used to resist the damaging effect of energetic plasma. For those samples with an a-Si thickness >20nm, the damage caused is insignificant.

Two sets of SIMS profiles, with and without ICNP treatment, are shown in Fig. 3 for comparison. In this case, there are two peaks in the nitrogen concentration, located at the poly-Si/oxide and oxide/Si interfaces. Comparing the profiles of boron in Fig. 3, it is found that the concentration of boron decreases more sharply in the substrate for the sample undergoing the ICNP treatment. The large increased amount of piled nitrogen in the gate/oxide and oxide/Si interface after the ICNP process implies that the reduction of boron penetration is strongly related to the population of nitrogen.

In conclusion, the suppression of boron penetration in the stacked poly-Si/a-Si gate structure by inductive-coupling-nitrogen-plasma is demonstrated. This novel approach provides a very small shift in the flat-band voltage and a large breakdown charge for pMOS devices. Better characteristics can be achieved by selecting the SAP structure with a 30nm a-Si layer undergoing the ICNP treatment.

Acknowledgments: The authors would like to express thanks for the financial support of the National Science Council of the Republic of China under contract NSC-84-2215-E-035-004. The technical support by the National Nano Device Laboratories is also acknowledged.

References


Integrated concave grating WDM demultiplexer with 0.144 nm channel spacing

Z.J. Sun, K.A. McGreer and J.N. Broughton

Indexing terms: Integrated optics, Grating demultiplexers, Wavelength division multiplexing

A 60-channel WDM demultiplexer based on a concave grating with 0.144nm channel spacing in the 1.5μm wavelength region was fabricated. The demultiplexer comprises SiO2/SiON/SiO2 waveguides on Si and an individual channel has a full width at half maximum spectral width of 0.09nm.