A New Criterion for TransientLatchup Analysis in Bulk CMOS

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Abstract—This paper describes a new criterion for transient latchup of p-n-p-n structures initiated by current pulses. Based upon the circuit-oriented model, the terminal currents and voltages of the transistors as a function of the pulsed triggering currents are characterized, and the charge storage within p-n-p-n structures is investigated. It is found that, to maintain the regeneration process, the change of charge stored in junction depletion capacitances of a p-n-p-n structure must be greater than a certain value independent of the triggering currents. Thus, the new criterion is constructed in terms of the constant charge storage within a p-n-p-n structure. Applying the criterion, latchup immunity against pulsed triggering currents can be evaluated with respect to process and device parameters. Both SPICE simulations and experimental results confirm the validity of the proposed transient criterion. It is found that large transit time of bipolar transistors and large well-substrate junction depletion capacitance lead to higher latchup immunity against pulsed triggering currents.

NOMENCLATURE

$C_{Jc}$ Collector junction capacitance.
$C_{Je}$ Emitter junction capacitance.
$HC$ Low-current compensation parameter of a bipolar transistor.
$I_{S}$ Reverse saturation current of a bipolar transistor.
$t_r$ Regeneration time of a p-n-p-n structure.
$V_T$ Thermal voltage.
$\beta_{F(R)}$ Ideal maximum forward (reverse) current gain of a bipolar transistor.
$\tau_{F(R)}$ Forward (reverse) transit time of a bipolar transistor.
$\theta$ High-level injection parameter of a bipolar transistor.
$\phi_p$ Built-in potential of a p-n junction.
$Q_1$ Lateral p-n-p transistor.
$Q_2$ Vertical n-p-n transistor.

I. INTRODUCTION

It is known that one of the main factors limiting the performance of VLSI CMOS circuits is latchup phenomenon, i.e., the triggering operation of parasitic p-n-p-n structures. According to either the holding-point [1]-[4] or triggering-point [5], [6] approach, a number of design models and simulation programs have been proposed to analyze the static latchup characteristics. In addition to these static models, a few models are devoted to characterizing the transient latchup behavior by two-dimensional numerical simulation or analytic modeling [7]-[11]. Although 2-D transient simulations provide more accurate analysis of latchup behavior, the rigorous calculations generally consume rather large computer time. Moreover, the lack of latchup criterion in 2-D simulation usually leads to a trial-and-error analysis in obtaining the triggering margin of a p-n-p-n structure. Therefore, definite criteria for latchup initiation in the transient case are required to make latchup analysis more meaningful.

Power-up ramp induced latchup has been analyzed [9], and it is shown that the well-substrate junction capacitance is important for understanding the power-up transient. On the other hand, an analytic model and transient criterion have been constructed in terms of transistor currents by Goto et al. [10]. However, using a piecewise linear model and neglecting junction and diffusion capacitances overestimates the transistor transient currents. Thus, the derived criterion in [10] is insufficient to accurately predict the dynamic triggering behavior of p-n-p-n structures.

In this paper, the transient behavior of p-n-p-n structures under external pulsed triggering currents is investigated in detail, and the new criterion for transient latchup initiation is established. Based upon the lumped equivalent model, the time-dependent terminal voltages and currents of the parasitic bipolar transistors are first analyzed in Section II where the effects of transistor transit time, diffusion capacitances, and bias-dependent junction capacitances are included. Based on the observation of charge storage rather than the variation of terminal currents in the p-n-p-n structures, a dynamic criterion for latchup initiation is proposed in Section III. From the proposed criterion, the relation between the minimum pulse width, or the regeneration time of the p-n-p-n structure, and the pulse height of triggering currents for latchup initiation can be obtained. Comparisons with SPICE simulation results confirm the validity of the proposed latchup criterion. Section IV gives the experimental results for various p-n-p-n structures. Good agreement between the experimental and theoretical results is obtained.

II. DYNAMIC BEHAVIOR OF THE P-n-p-n STRUCTURE

To simplify the analysis and get an insight into the dynamic operation, the latchup behavior is characterized through the conventional two-transistor model. Fig. 1 shows the lumped equivalent model for the p-n-p-n struc-
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Fig. 1. Lumped equivalent circuit for modeling the transient behavior of the p-n-p-n structure.

In p-well technology, Q1 is the lateral p-n-p transistor and Q2 is the vertical n-p-n transistor. Rf and R2 represent the corresponding well and substrate shunt resistances across the base node of transistors Q2 and Q1, where the pulsed triggering currents I2 and I1 are also applied. Other components are the bias-dependent junction capacitances. Note that the capacitances Cj1c and Cj2c are the well-substrate junction capacitances, which play an important role in transient latchup as will be shown later.

In the transient case, the displacement currents through the junction capacitances and diffusion capacitances of Q1 and Q2 are so significant that they must be considered. Thus, taking the effects of junction depletion capacitance and diffusion capacitance into consideration, the transient terminal currents of Q1 and Q2 can be written as [12]

\[ i_{c1}(t) = I_{C1} - (C_{j1c} + C_{F1}) \frac{d(V_{CE1} + V_{EB1})}{dt} \]

(1)

\[ i_{b1}(t) = I_{B1} + (C_{j1c} + C_{F1}) \frac{d(V_{EB1} + V_{CE1})}{dt} + (C_{j1c} + C_{R1}) \]

(2)

\[ i_{c2}(t) = I_{C2} - (C_{j2c} + C_{F2}) \frac{d(V_{BE2} - V_{CE2})}{dt} \]

(3)

\[ i_{b2}(t) = I_{B2} + (C_{j2c} + C_{F2}) \frac{d(V_{BE2} - V_{CE2})}{dt} + (C_{j2c} + C_{R2}) \]

(4)

where

\[ C_{F1} = \frac{(I_{S10} \tau_{F1} / V_F)}{e^{V_{EB1}/V_T}} \]

(5)

and

\[ C_{R1} = \frac{(I_{S10} \tau_{R1} / V_F)}{e^{V_{CE1} + V_{EB1}/V_T}} \]

(6)

I_{C1}, I_{B1}, I_{C2}, and I_{B2} in (1)-(4) are the static transistor currents of Q1 and Q2. These currents are related to the transistor terminal voltages as expressed in Appendix A. The diffusion capacitances C_{F2} and C_{R2} have similar expressions to C_{F1} and C_{R1}, respectively, which are derived by assuming constant transistor transit times \( \tau_{F1} \) and \( \tau_{R1} \) (i = 1, 2). Moreover, the junction depletion capacitances C_{j1c} and C_{j2c} (i = 1, 2) in (1)-(4) are also bias dependent and are further expressed in Appendix B.

From the circuit of Fig. 1, the relations between the terminal currents and voltages can be written as

\[ i_{c2} - i_{b1} + V_{EB1}/R_2 + I_1 = 0 \]

(7)

\[ i_{c1} - i_{b2} - V_{BE2}/R_1 + I_2 = 0 \]

(8)

and

\[ V_{CE1} = V_{BE2} - V_{DD} \]

(9)

\[ V_{CE2} = V_{DD} - V_{EB1} \]

(10)

Substituting (1)-(4) into (7) and (8), and using (9) and (10), the dynamic behavior of the base-emitter voltages \( V_{EB1} \) and \( V_{BE2} \) can be obtained as

\[ \frac{dV_{EB1}}{dt} = - \frac{I_{D1} C_2 + I_{D2} (C_{j1c} + C_{j2c})}{(C_{j1c} + C_{j2c}) C_T} \]

(11)

and

\[ \frac{dV_{BE2}}{dt} = \frac{I_{D2} C_1 - I_{D1} (C_{j1c} + C_{j2c})}{(C_{j1c} + C_{j2c}) C_T} \]

(12)

where

\[ C_1 = C_{j1c} + C_{F1} + C_{F1} + C_{R1} \]

(13)

\[ C_2 = - (C_{j1c} + C_{j2c} + C_{j2c} + C_{F2}) \]

(14)

\[ I_{D1} = V_{EB1}/R_2 - I_1 - I_{C2} + I_{B1} \]

(15)

\[ I_{D2} = I_{B2} + V_{BE2}/R_1 - I_{C1} - I_2 \]

(16)

and

\[ C_F = (C_{j1c} + C_{F1})(C_{j2c} + C_{F2})/(C_{j1c} + C_{j2c}) \]

\[ - (C_{j1c} + C_{j2c} + C_{F1} + C_{F2}) \]

(17)

In (13), (14), and (17), the reverse diffusion capacitances C_{F1} and C_{R2} are neglected as compared with the junction depletion capacitances C_{j1c} and C_{j2c}. Using (11) and (12), the variations of \( V_{EB1}(t) \) and \( V_{BE2}(t) \) with respect to both pulsed triggering current \( I_1 \) or \( I_2 \) and device parameters can be obtained numerically.

Fig. 2(a) shows the calculated results of \( V_{EB1}(t) \) and \( V_{BE2}(t) \) for different pulse widths of \( I_1 \) with a fixed pulse height equal to 5 mA. The device parameters used are
listed in Table I with $R_1 = 5.6 \, \text{k}\Omega$ and $R_2 = 800 \, \Omega$. As can be seen from Fig. 2(a), $V_{EB1}$ increases sharply when $I_1$ is applied. The sharp increase of $V_{EB1}$ corresponds to a sharp decrease of voltage at the base node of $Q_1$. Thus, due to the capacitive coupling effect caused by $C_{J1}$ and $C_{J2}$, $V_{BE2}$ decreases below 0 V during the initial period and thereafter is increased by the increase of $I_{C1}$. When $I_1$ drops to zero at $t = 5 \, \text{ns}$, $V_{EB1}$ decreases whereas $V_{BE2}$ continues to increase for some time (dashed curves), still due to the coupling effect of $C_{J1}$ and $C_{J2}$. However, because of the insufficiently large pulse width of $I_1$, the regeneration of the p-n-p-n structure cannot be maintained, and both $V_{EB1}$ and $V_{BE2}$ finally decrease to zero, as shown in Fig. 2(a). When the pulse width increases from 5 to 10 ns, the p-n-p-n structure is triggered into latchup, as can be seen from the values of $V_{EB1}$ or $V_{BE2}$ (solid curves), which remain at their turn-on value ($\approx 0.8 \, \text{V}$) after $I_1$ is removed.

Fig. 2(b) shows the calculated $V_{BE2}(t)$ and $V_{EB1}(t)$ for different pulse widths of $I_2$ with a fixed pulse height equal to 5 mA. Similarly, an initial delay time is seen for $V_{EB1}(t)$ and the pulse width must be sufficiently large to trigger the p-n-p-n structure into latchup.

The variations of terminal currents $I_{B1}(t)$, $I_{C1}(t)$, $I_{B2}(t)$, $I_{C2}(t)$, $I_{B1}(t) = V_{EB3}(t)/R_1$, and $I_{B2}(t) = V_{EB1}(t)/R_2$ calculated from (A1)–(A4) for the 5-mA pulse height of $I_1$ and $I_2$ are shown in Fig. 3(a) and (b), respectively. We define the regeneration time $t_1$, as the required minimum pulse width of a fixed pulse height of $I_1$ or $I_2$ such that the regeneration process of the p-n-p-n structure can be maintained after $I_1$ or $I_2$ is removed. The value of $t_1$ obtained from SPICE simulations is marked by
Fig. 3. Variation of the branch currents of the p-n-p-n structure in transient case for 5-mA pulse height of (a) $I_1$ and (b) $I_2$ applied.

TABLE I

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$Q_1$(PNP)</th>
<th>$Q_2$(NPN)</th>
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<td>$f_p$</td>
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<tr>
<td>$j_R$</td>
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<tr>
<td>$I_0$(A)</td>
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<td>8.112E-16</td>
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<td>$\theta$</td>
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<td>1.291E-6</td>
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<td>$t_p$(ns)</td>
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</tr>
<tr>
<td>$t_R$(ns)</td>
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<td>2.0</td>
</tr>
<tr>
<td>$C_{JC}$(pf)</td>
<td>2.0</td>
<td>0.6</td>
</tr>
<tr>
<td>$C_{JE}$(pf)</td>
<td>0.6</td>
<td>1.3</td>
</tr>
<tr>
<td>$R_C$</td>
<td>150</td>
<td>150</td>
</tr>
</tbody>
</table>

As can be seen from Fig. 3, all the currents increase drastically during the regeneration process and approach constant values as the p-n-p-n structure enters the stable latchup state [6]. However, at $t = t_r$, the current $I_{C2}$ is much smaller than the current ($I_{R1} + I_{R2}$) while $I_{C1}$ is much larger than ($I_{R2} + I_{R1}$), as shown in Fig. 3(a) for $I_1$ triggering. Similarly, as shown in Fig. 3(b) for $I_2$ triggering, the current $I_{C2}$ at $t = t_r$ is much larger than the current ($I_{R1} + I_{R2}$) whereas $I_{C1}$ is much smaller than ($I_{R2} + I_{R1}$). These unbalanced terminal currents of $Q_1$ and $Q_2$ at $t = t_r$ are mainly caused by the effects of displacement currents through the junction depletion capacitances and diffusion capacitances during the regeneration process. Note that due to the high-injection effect of $Q_1$, the current gain of $Q_1$ may be smaller.
than 1 and $I_{B1}$ may be larger than $I_{C1}$ accordingly as shown in Fig. 3. From Fig. 3(a) and (b), it is concluded that, to initiate the regeneration process of the p-n-p-n structure, the current $I_{C1}$ ($I_{C2}$) is not necessarily larger than or equal to $(I_{B2} + I_{R1})/(I_{B1} + I_{R2})$ at $t = t_r$ in the $I_2(I_1)$ triggering case.

III. DYNAMIC LATCHUP CRITERION

From the above discussion, it is realized that the displacement currents of junction depletion capacitances have strong effects on the dynamic behavior of p-n-p-n structures. As the triggering current is applied, the base-emitter voltage of $Q_1$ and $Q_2$ varies according to (11) and (12) such that the charges stored in the junction depletion capacitances are redistributed. Due to this charge redistribution, the terminal currents of $Q_1$ and $Q_2$ must adjust to maintain charge conservation at the base node of $Q_1$ or $Q_2$.

By taking an average value for the junction depletion capacitances to neglect the variations of junction depletion capacitances with voltage, the charge $q_1(t)$ stored at the junction depletion capacitance connected to the base node of $Q_1$ can be written as

$$q_1(t) = \bar{C}_{j1}V_{EB1}(t) + (\bar{C}_{j1} + \bar{C}_{j2}) \left[ V_{BE2}(t) - V_{DD} + V_{EB1}(t) \right]$$

whereas that connected to the base node of $Q_2$ is

$$q_2(t) = -\bar{C}_{j2}V_{BE2}(t) + (\bar{C}_{j1} + \bar{C}_{j2}) \left[ V_{DD} - V_{EB1}(t) - V_{BE2}(t) \right]$$

where $\bar{C}_{ji}$ and $\bar{C}_{j2}$ ($i = 1, 2$) are the average junction depletion capacitances, as expressed in Appendix B. Note that both $q_1(t)$ and $q_2(t)$ do not include the charge stored in the diffusion capacitances. With the initial values of $V_{EB1}(0) = 0$ and $V_{BE2}(0) = 0$, the incremental changes of $q_1$ and $q_2$ with time can be written from (18) and (19) as

$$\Delta q_1(t) = q_1(t) - q_1(0) = (\bar{C}_{j1} + \bar{C}_{j1} + \bar{C}_{j2})V_{EB1}(t) + (\bar{C}_{j1} + \bar{C}_{j2})V_{BE2}(t)$$

and

$$\Delta q_2(t) = q_2(t) - q_2(0) = -(\bar{C}_{j2} + \bar{C}_{j1} + \bar{C}_{j2})V_{BE2}(t) + (\bar{C}_{j1} + \bar{C}_{j2})V_{EB1}(t).$$

Applying (20) and (21), Fig. 4(a) shows the calculated variations of $\Delta q_1(t)$ for different values of pulse height of $I_1$. For each pulse height of $I_1$, the corresponding $t_r$ obtained from SPICE simulations is also marked in Fig. 4(a) by an arrow. As can be seen from Fig. 4(a), $\Delta q_1$ increases with time as the triggering current $I_1$ is applied and approaches a limiting value as the p-n-p-n structure enters the stable latchup state. At $t = t_r$, however, the value of $\Delta q_1$ remains unchanged for different pulse heights of $I_1$, as shown in Fig. 4(a). Similarly, the magnitude of the charge $\Delta q_2$ calculated from (21) for various pulse heights of $I_2$ is shown in Fig. 4(b) where $\Delta q_2$ is also unchanged at $t = t_r$. The results of Fig. 4 reveal that the regeneration time can be obtained from the change of charge stored in the junction depletion capacitances connected to the base node of $Q_1$ or $Q_2$.

Denoting the charge $\Delta q_1$ ($\Delta q_2$) at $t = t_r$ as $\Delta q_{1r}$ ($\Delta q_{2r}$), the constant $\Delta q_{1r}$ or $\Delta q_{2r}$, can be physically interpreted as follows. When $I_1$ ($I_2$) is applied to the base node of $Q_1$ ($Q_2$), a net charge $\Delta q_{1r}$ ($\Delta q_{2r}$) is stored in the junction depletion capacitances connected to the base node of $Q_1$ ($Q_2$). As long as $\Delta q_{1r}$ ($\Delta q_{2r}$) increases to a certain value $\Delta q_{1r}^*$ ($\Delta q_{2r}^*$), independent of $I_1$ ($I_2$), the stored charge $\Delta q_{1r}$ ($\Delta q_{2r}$) is large enough to sustain the regeneration of the p-n-p-n structure even when $I_1$ ($I_2$) is removed at $t = t_r$. To obtain $\Delta q_{1r}$ for a given p-n-p-n structure, one can obtain $t_r$ for an arbitrarily chosen pulse height of $I_1$ by SPICE simulations or exact numerical methods. After the value of $t_r$ is obtained, the variation of $\Delta q_{1r}$ ($\Delta q_{2r}$) is calculated from (11), (12), and (20). The calculated $\Delta q_{1r}$ at $t = t_r$ is then the value of $\Delta q_{1r}$. Similarly $\Delta q_{2r}$, can be calculated. Since the value of $\Delta q_{1r}$ ($\Delta q_{2r}$) is independent of applied pulse heights of $I_1$ ($I_2$) for a given p-n-p-n structure, they can be used to characterize transient latchup without any other trial and error.

Based upon the above observations, the dynamic latchup criterion for the p-n-p-n structure can be stated as:

1) for the triggering current $I_1$, the change of charge $q_1$ at the base node of $Q_1$ should be at least the value $\Delta q_{1r}$; or
2) for the triggering current $I_2$, the change of charge $q_2$ at the base node of $Q_2$ should be at least the value $\Delta q_{2r}$.

The calculation procedure for obtaining the regeneration time $t_r$ is:

a) For an arbitrary pulse height of $I_1$ ($I_2$), obtain $t_r$ by SPICE simulations or exact numerical methods.

b) Determine $\Delta q_{1r}$ ($\Delta q_{2r}$) by using (20) ((21)) and $t_r$ obtained in a).

c) For all the pulse heights of $I_1$ ($I_2$), calculate each $t_r$ by using the above criterion.

IV. RESULTS AND DISCUSSION

To verify the proposed criterion, the regeneration time $t_r$ is calculated by using the above procedure for different pulse heights of $I_1$ and $I_2$ and compared to that obtained from SPICE simulations. The results are shown in Fig. 5 where the adopted device parameters are shown in Table I with $\Delta q_{1r}$ ($\Delta q_{2r}$) found to be 1.49 pC (2.59 pC). As can be seen from Fig. 5, good agreement is obtained be-
tween theoretical and SPICE simulated results. This substantiates the validity of the dynamic latchup criterion.

It is seen from (20) and (21) that $\Delta q_1$ or $\Delta q_2$ (thus $\Delta q_{1r}$ or $\Delta q_{2r}$) are linearly proportional to the average collector junction depletion capacitance ($C_{jCB} + C_{jC2}$). Therefore, from the proposed latchup criterion, the regeneration time $t_r$ is also expected to be linearly proportional to ($C_{jCB} + C_{jC2}$). Fig. 6 shows the variations of calculated and SPICE simulated $t_r$ with different zero-biased collector junction depletion capacitances. As can be seen from Fig. 6, the regeneration time indeed increases linearly with the increase of the collector junction depletion capacitance, which corresponds to the well-substrate junction depletion capacitance. Thus, in contrast to the results of power-up ramp induced latchup [9], larger well-substrate junction depletion capacitance leads to larger regeneration time and higher latchup immunity against pulsed triggering currents.

Fig. 7(a) and (b) shows the variations of $t_r$ with forward transit times of $Q_1$ and $Q_2$ for 5-mA pulse height of $I_2$ and $I_1$, respectively. As the current $I_2$ is applied to the base of $Q_2$, the forward transit time of $Q_2$ has a stronger effect on $t_r$ than that of $Q_1$ and $t_r$ increases drastically as $\tau_{F2}$ increases. However, $\tau_{F1}$ has a limited effect on the increase of $t_r$, as can be seen from Fig. 7(a). The asymmetry in the sensitivity of $t_r$ to $\tau_{F1}$ and $\tau_{F2}$ results because the increase of $\Delta q_2(t)$ becomes much slower when $\tau_{F2}$ is increased, as compared with that when $\tau_{F1}$ is increased.
Therefore, increasing the forward transit time $\tau_{F1}$ of the lateral p-n-p transistor results in a limited effect on the transient latchup immunity against the well triggering current. For the current $I_1$ applied to the base of $Q_1$, both the increases of $\tau_{F1}$ and $\tau_{F2}$ lead to the increase of $t_r$, but $\tau_{F1}$ has a stronger effect on increasing $t_r$, as shown in Fig. 7(b).

The effects of substrate and well resistances on $t_r$ are shown in Fig. 8(a) and (b) under $I_1$ and $I_2$ triggerings, respectively. The decrease of $R_1$ or $R_2$ leads to an increase of $t_r$. However, because of the small current gain and large transit time of the lateral p-n-p transistor, which results in a slower increase of $\Delta q_l$ with time, the increase of $t_r$ due to the decrease of $R_2$ or $R_1$ in the $I_2$ triggering case is much
smaller than that in the $I_1$ triggering case, as can be seen in Fig. 8(a) and (b). This reveals that the efforts of decreasing the substrate resistance $R_2$ have a limited effect on the transient latchup immunity against the pulsed well triggering current. It should be noted that the decrease of $R_1$ or $R_2$ also increases the value of the static well and substrate triggering currents so that latchup immunity is greatly enhanced [6]. However, as long as the pulse height of the triggering current exceeds the static triggering current, the decrease of $R_1$ or $R_2$ becomes more effective in increasing the regeneration time of $I_1$ than that of $I_2$ in the transient case. Moreover, as shown in Fig. 8, the variation of $t_s$ is more sensitive to $R_2$ ($R_1$) than to $R_1$ ($R_2$) for the case of $I_1$ ($I_2$) triggering current, similar to the results in [10].

The results of Figs. 7 and 8 show that the sensitivity of $t_s$ to the parameters of $Q_1$ and $Q_2$ depends also on whether the applied pulsed triggering current is a well triggering current or a substrate triggering current. When the well triggering current $I_2$ is applied to the base node of $Q_2$, the
well resistance $R_1$ and the parameters of $Q_2$ have larger effects on $t_r$ than the substrate resistance $R_2$ and the parameters of $Q_1$. Similarly, $t_r$ has a higher sensitivity to the substrate resistance $R_2$ and the parameters of $Q_1$ when the substrate triggering current $I_2$ is applied.

**V. EXPERIMENT**

A p-n-p-n test pattern was designed and fabricated by using the 2-$\mu$m p-well technology to investigate the dynamic triggering characteristics of latchup. The surface concentration of the p-well was $1 \times 10^{16}$ cm$^{-3}$ and the resistivity of the n-substrate was 2–3 $\Omega$-cm. The spacing between n$^+$ and p$^+$ regions in the well was 30, 70, or 170 $\mu$m whereas that in the substrate was 40 or 180 $\mu$m. The resistance $R_1$ or $R_2$ varies with the n$^+$ to p$^+$ spacing in the well or substrate. With a 5-V power supply, current pulses with different pulse widths and pulse heights were applied to the n$^+$ region in the substrate or p$^+$ region in the well as the triggering current. At the instant latchup occurred, the pulse width was measured as the regeneration time $t_r$.

In the theoretical calculation, the base–emitter voltages $V_{EB1}(t)$ and $V_{BE2}(t)$ are calculated from (11) and (12) or from SPICE simulations for each pulse height by using the device parameters in Table II. The values of $\Delta q_1$ and
\[ \Delta q_2 \text{ are then calculated from the calculated } V_{EB_1}(t) \text{ and } V_{BE_2}(t) \text{ by using (20) and (21). The regeneration time is thus calculated as the time at which } \Delta q_1(\Delta q_2) \text{ is equal to } \Delta q_{1r}(\Delta q_{2r}). \]

Fig. 9(a) shows the calculated and experimental results of \( t_r \) for various pulse heights of \( I_2 \) with \( R_1 \) as a parameter. The values of the corresponding measured static \( I_2 \) triggering current from the same structure are also shown in Fig. 9(a) by solid symbols. For the calculated \( \Delta q_2 \), shown in Fig. 9(a), good agreement is obtained between theoretical and experimental results. As can be seen from Fig. 9(a), \( t_r \) increases with the decrease of the pulse height of \( I_2 \) and drastically increases with the decrease of \( R_1 \). Moreover, for large values of \( t_r \), the value of the pulse height of \( I_2 \) approaches to that of the corresponding static trig-

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### TABLE II

**DEVICE PARAMETERS OF BIPOLAR TRANSISTORS IN THE EXPERIMENTAL TEST PATTERN**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>( Q_1 ) (PNP)</th>
<th>( Q_2 ) (NPN)</th>
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<tr>
<td>( f_p )</td>
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<tr>
<td>( f_p )</td>
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<td>( I_{c_2} ) (A)</td>
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<td>( \beta )</td>
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<td>4.0E-6</td>
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<tr>
<td>( t_{p_2} ) (ns)</td>
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<td>( C_{jc} ) (pf)</td>
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<td>( C_{je} ) (pf)</td>
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</tbody>
</table>
gerring current as expected. The experimental and calculated results of \( t_\text{r} \), for various pulse heights of \( I_\text{p} \), and the measured value of \( I_\text{p} \) in the static triggering case are shown in Fig. 9(b), where good agreement is also obtained.

VI. CONCLUSION

The dynamic triggering characteristics of the p-n-p-n structure are described. The junction depletion capacitances of parasitic bipolar transistors are found to have significant effects on the transient variations of transistor terminal currents and voltages. Moreover, the charge stored in junction depletion capacitances of a p-n-p-n structure must be larger than some threshold value to maintain the regeneration of the p-n-p-n structure that leads to latchup. This threshold value is found to be independent of the pulse height of the applied triggering currents. The dynamic latchup criterion, therefore, is constructed in terms of the constant charge-storage within the p-n-p-n structure. Both SPICE simulation and experimental results show the validity of the proposed criterion. It is found that large forward transit times of parasitic bipolar transistors and large well-substrate junction depletion capacitances lead to the long regeneration time required for sustaining the regeneration of a p-n-p-n structure and thus high latchup immunity against pulsed triggering currents.

APPENDIX A

Taking both the high-level injection effect and the surface leakage current effect into consideration, the static terminal currents of both transistors can be written as [12]

\[
I_{B1} = (I_{S10}/\beta_{R1})(e^{V_{BE1}/V_T} - 1) + (I_{S10}/\beta_{R1})e^{V_{BE1}/V_T} \cdot e^{(V_{BE1} + V_{CE1})/V_T - 1} + HC_{I1}I_{S10}(e^{V_{BE1}/2V_T} - 1)
\]

\[
I_{C1} = I_{S1}e^{V_{BE1}/V_T}(1 - e^{V_{CE1}/V_T}) - (I_{S1}/\beta_{R1})[e^{(V_{BE1} + V_{CE1})/V_T - 1}]
\]

\[
I_{B2} = (I_{S20}/\beta_{R2})e^{V_{BE2}/V_T} - 1 + (I_{S20}/\beta_{R2})e^{V_{BE2}/V_T} \cdot e^{(V_{BE2} - V_{CE2})/V_T - 1}

+ HC_{I2}I_{S20}e^{V_{BE2}/2V_T - 1}
\]

\[
I_{C2} = I_{S2}e^{V_{BE2}/V_T}[1 - e^{-(V_{CE2}/V_T)}]

- (I_{S2}/\beta_{R2})[e^{(V_{BE2} - V_{CE2})/V_T - 1}]
\]

where

\[
I_{S1} = I_{S10}/(1 + \theta_1 e^{V_{BE1}/2V_T})
\]

and

\[
I_{S2} = I_{S20}/(1 + \theta_2 e^{V_{BE2}/2V_T}).
\]

APPENDIX B

The collector and emitter junction depletion capacitances in (1) to (4) can be written, respectively, as

\[
C_{j1} = C_{j10}/[1 - (V_{BE2} + V_{EB1} - V_{DD})/\phi_b]^{1/3}
\]

\[
C_{j2} = C_{j20}/[1 - (V_{BE2} + V_{EB1} - V_{DD})/\phi_b]^{1/3}
\]

for graded junctions and

\[
C_{j1} = C_{j10}/(1 - V_{EB1}/\phi_b)^{0.5}
\]

\[
C_{j2} = C_{j20}/(1 - V_{EB2}/\phi_b)^{0.5}
\]

for abrupt junctions.

The average junction depletion capacitances \( \overline{C}_{j1} \) and \( \overline{C}_{j2} \) can be written from (B1) and (B3) as

\[
\overline{C}_{j1} = \frac{3C_{j10}\phi_b}{2(V_{DD} - V_{BE20} - V_{EB10})}\left[1 + \frac{V_{DD}^{2/3}}{\phi_b}\right]

- \left(1 + \frac{V_{DD} - V_{BE20} - V_{EB10}}{\phi_b}^{2/3}\right)\right]^{1/3}
\]

and

\[
\overline{C}_{j2} = \frac{2\phi_bC_{j20}}{V_{EB10}}\left[1 - \left(1 - \frac{V_{EB10}}{\phi_b}\right)^{0.5}\right]^{1/3}
\]

where \( V_{EB10} \) and \( V_{BE20} \) are the corresponding cut-in voltages \((\approx 0.55 \text{ V})\) of the base-emitter junctions of \( Q_1 \) and \( Q_2 \), respectively. \( \overline{C}_{j12} \) and \( \overline{C}_{j22} \) have similar expressions.

REFERENCES


*  

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