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Improvement of Polysilicon Oxide Integrity Using NF₃-Annealing

Wen Luh Yang, Ming Sun Shieh¹, Yu Min Chen, Tien Sheng Chao²,
Don-Gey Liu and Tan Fu Lei¹

Institute and Department of Electrical Engineering, Feng Chia University, Taichung, Taiwan, R.O.C.
¹Institute and Department of Electronics, National Chiao Tung University, Hsinchu, Taiwan, R.O.C.
²National Nano Device Laboratories, Hsinchu, Taiwan, R.O.C.

(Received April 7, 2000; accepted for publication May 19, 2000)

We report a method to improve the polysilicon oxide integrity by using NF₃-annealing. Incorporating with stronger Si–N and Si–F bonds at the polysilicon/polyoxide interface, significant improvements are found in terms of roughness, breakdown strength, charge-to-breakdown, and stress-induced-leakage-current.

KEYWORDS: polyoxide, NF₃-annealing, nitrogen, fluorine, SILC

1. Introduction

For nonvolatile memories such as eraseable-programmable read-only memory (EPROM), electrical-erasable programmable read-only memory (EEPROM), and Flash, thermal oxides grown on n⁺ polysilicon (polyoxides) have been used as the interdielectrics. Requirements of the polyoxides include low leakage current and high electric breakdown field (Ebd) to achieve a long charge retention time. However, polyoxides exhibit lower breakdown field and higher leakage current than oxides grown on single crystal silicon due to surface roughness caused by the enhanced oxidation at polysilicon grain boundaries. Recent studies show that the reliability of MOS and polyoxide capacitors can be improved by introducing proper amounts of fluorine.¹–³) It also reported that the N₂O-grown and N₂O-annealing polyoxides have better electrical performance than O₂-grown polyoxide, which attributes to the nitrogen incorporation at the polysilicon/polyoxide interface.⁴,⁵) Therefore, in this paper, NF₃-annealing is proposed to achieve the advantages of both nitrogen and fluorine simultaneously. By using optimized NF₃ flow-rate, it can be expected to improve the polyoxide integrity. As compared to the ion-implantation, this method provides a low cost and high throughput for mass production.

2. Experimental

The n⁺–polysilicon/polyoxide/n⁺–polysilicon capacitors were fabricated on the p-type (100) silicon wafers. First, a 100 nm-thick buried oxide was thermally wet oxidized at 1000°C. Then the polysilicon layer (bottom polysilicon) with a thickness of 300 nm was deposited and subsequently doped with POCl₃ at 875°C to obtain a sheet resistance of 40–60 Ω/□. The p-glass was stripped off and then an 83 Å polyoxide was grown at 900°C in dilute (N₂ + O₂) ambient. After that, a 300 nm-thick top polysilicon layer was deposited, followed by annealing in the diluted NF₃ gas. Samples were annealed in NF₃ at 600°C with pressure of 260 mTorr for different time, 10 to 30 minutes in a low-pressure chemical-vapor-deposition (LPCVD) system. After optimization, the flow rates for N₂ and NF₃ were set at 200 and 3 sccm, respectively. Then top polysilicon was doped by POCl₃ as the n⁺–polysilicon gate electrode at 875°C for 1 hour. After defining the top gate pattern, a passivation oxide was deposited by plasma enhanced chemical vapor deposition (PECVD) and contact holes were opened. Finally, Aluminum was sputtered, patterned, and sintered at 350°C for 40 minutes.

3. Results and Discussion

Figure 1 shows curves of current density vs electric field. The electric field is defined as Vg/Tox, where Vg is the gate voltage. The breakdown field, Ebd, increases with the introduction of NF₃-annealing, which reaches a maximum of 15 MV/cm for 20 minutes case. The inset in Fig. 1 shows the root-mean-square roughness measured by the atomic force microscope (AFM) of bottom polysilicon with different NF₃-annealing time. The value of surface roughness decreases as introduction of NF₃ and reaches to a minimum for 20-min annealing. These results show that 20-min annealing is the optimized condition to obtain the smoothest surface of the bottom polysilicon, and results in a highest Ebd in return. For a longer annealing time, i.e., 30-min, excessive fluorine and/or nitrogen atoms break the Si–O–Si bonds and create non-bridging oxygen defects. Figure 2 shows gate voltage shift under constant current stressing at 100 μA/cm² for these four samples. NF₃-annealing samples show a smaller charge trapping-rate than control sample. This implies NF₃-annealing samples have better immunity to electron trapping than control.

As considering the reliability of polyoxide in nonvolatile memories, charge-to-breakdown (Qbd) is to guaranty long read/write cycles. In the conventional polyoxide fabrication, Qbd values are very small (in the range of 0.01 to 0.1 C/cm²)

![Fig. 1. The J-E characteristics of polyoxides with/without NF₃ annealed for positive top-gate bias. The inset is surface roughness for these four samples.](image-url)
due to surface roughness and non-uniform polyoxide thickness. Figure 3 shows the $Q_{bd}$ for these four samples. With NF$_3$ treatments, $Q_{bd}$ increases significantly. Besides the improvement on roughness as mentioned in Fig. 1, the improved integrity is also due to incorporation of nitrogen and fluorine atoms which relax the interface stress.\(^2\) It is found that $Q_{bd}$ greater than 1 C/cm$^2$ can be obtained as NF$_3$ annealing time is larger than 20-min. Finally the stress-induced-leakage-current (SILC) was investigated. Mechanism of SILC could be explained by the stress-induced weak spots with a lowering barrier height, the trap-assisted tunneling by the neutral electron trap filling and emptying, and the positive charge assisted tunneling.\(^5\)–\(^8\) The fresh and the after stressed $I$–$V$ curves are shown in Fig. 4. It is seen that the SILC of the NF$_3$-annealing sample was smaller than that of the control sample. Once again, the stronger Si–F and Si–N bonds at the polysilicon/polyoxide interface resulting from the NF$_3$ annealing made polyoxides less vulnerable than the control sample under the electrical stressing. In this study, all samples were measured with the positive-gate bias and the results of the negative-gate bias were similar to those obtained from the positive-gate bias.

4. Conclusions

NF$_3$-annealing method had been demonstrated to improve the polyoxide integrity. The breakdown field up to 15 MV/cm and charge-to-breakdown more than 1 C/cm$^2$ can be obtained using NF$_3$-annealing. Incorporating with stronger Si–N and Si–F bonds at the polysilicon/polyoxide interface, significant improvements are found in terms of roughness, breakdown strength, charge-to-breakdown, and stress-induced-leakage-current.

Acknowledgement

The authors would like to express thanks for the financial support of the Feng Chia University through the contract of FCU-RD-88-01. The partial financial support of the National Science Council of the R.O.C. (NSC-89-2215-E-035-010) is also acknowledged.