Improved Low Temperature Characteristics of P-Channel MOSFETs with Si$_{1-x}$Ge$_x$ Raised Source and Drain

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Abstract—P-channel metal–oxide–semiconductor field-effect transistors with Si$_{1-x}$Ge$_x$ raised source and drain (RSD) have been fabricated and further studied for low temperature applications. The Si$_{1-x}$Ge$_x$ RSD layer was selectively grown by ANELVA SRE-612 ultra-high vacuum chemical vapor deposition (UHVCD) system. Compared to devices with conventional Si RSD, improved transconductance and specific contact resistance were obtained, and these improvements become even more dramatic with reducing channel length. Well-behaved short channel characteristics with reduced drain-induced barrier lowering (DIBL) and off-state leakage current are demonstrated on devices with 100 nm Si$_{1-x}$Ge$_x$ RSD, due to the resultant shallow junction and less implantation damage. Moreover, temperature measurements reveal that Si$_{1-x}$Ge$_x$ RSD devices show more dramatic improvement in device performance at low temperature (<50 °C) operation, which can be ascribed to the higher temperature sensitivity of the Si$_{1-x}$Ge$_x$ sheet resistance.

Index Terms—Low temperature measurements, PMOSFET, selective epitaxial growth (SEG), short channel effect, strained-SiGe, ultra-high vacuum chemical vapor deposition.

I. INTRODUCTION

TO MEET the stringent demand of sub-0.1 μm devices, shallow junctions fabricated by out-diffusion from an in situ doped or ion-implanted p+/n+ Si$_{1-x}$Ge$_x$ layer have been reported [1]–[4]. Previously, pure Si selective epitaxy has been proposed to form elevated source/drain (also known as raised source/drain) metal oxide semiconductor field effect transistor (MOSFET) to simultaneously achieve shallow junction for better device operation, and a thick sacrificial layer for reliable silicided contact to the junction [5]–[9]. In these regards, Si$_{1-x}$Ge$_x$ is better suited than pure Si. Si$_{1-x}$Ge$_x$ can not only be selectively deposited onto the exposed source and drain (S/D) area, similar to pure Si, it also enjoys a lower deposition temperature, which is beneficial for device application. Besides, Si$_{1-x}$Ge$_x$ can be selectively etched with high selectivity to Si and SiO$_2$ [10]. More importantly, Si$_{1-x}$Ge$_x$ has a lower Schottky barrier height with respect to p$^+$ junction because of the reduced band gap, which results in a lower contact resistivity and higher current drive, when compared to pure Si [11]–[13]. Recently, we have successfully fabricated p-channel metal oxide semiconductor field effect transistor (PMOSFET) with Si$_{1-x}$Ge$_x$ as the raised S/D layer, and its impacts on contact resistance and device performance have been studied [13]. In particular, we showed that by employing Si$_{0.85}$Ge$_{0.14}$ RSD, a drive current (measured at $V_D = -2.5$ V and $V_G = -V_T = -2.5$ V) of 246 μA/μm, which represents a 17% improvement, compared to the counterpart with pure Si RSD, is achieved for an effective channel length of 0.24 μm. Furthermore, the improvement is found to increase with reducing channel length. For example, the improvement is only 15% when $L_{eff} = 0.5$ μm. However, the improvement can reach 29% when $L_{eff}$ is reduced to 0.16 μm. This demonstrates the importance of maintaining a low series resistance as device is scaled down, thus makes the device with Si$_{0.85}$Ge$_{0.14}$ RSD even more attractive for future sub-0.1 μm technologies.

In this work, we report, for the first time, the temperature dependence on the Si$_{1-x}$Ge$_x$ RSD device performance. Detailed electrical characteristics of PMOSFETs with and without various RSD structures were measured and compared at three different temperatures, i.e., room temperature, −50 °C, and 100 °C. In addition, the drain-induced barrier lowering (DIBL) characteristics of PMOSFETs with Si$_{1-x}$Ge$_x$ RSD and the specific contact resistivity and sheet resistance variation as a function of temperature were also studied in detail.

II. EXPERIMENTS

The fabrication of P-channel MOS transistors with various raised source/drain structures started with a standard baseline process [13]. Briefly, following a 4 nm gate oxide growth and polysilicon gate formation, source/drain extension implant ($1 \times 10^{15}$ cm$^{-2}$, 10 KeV) was performed. Then, a 800 °C, 20 min furnace anneal and a 1050 °C, 10 s rapid thermal anneal
(RTA) were performed for dopant activation. Afterwards, a 150 nm sidewall spacer was formed. Next, wafers were split to receive either SiGe or Si selective epitaxial growth (SEG) on the exposed S/D regions by an ANELVA SRE-612 cold-wall ultra-high vacuum chemical vapor deposition (UHVCVD) system [14]. The standby base pressure was kept at $2 \times 10^{-10}$ torr. For growing B-doped strained Si$_{1-x}$Ge$_x$ layers, Si$_2$H$_6$, GeH$_4$, and 1% B$_2$H$_6$ diluted in H$_2$ were introduced to achieve a growth rate of 41 Å/min for Si$_{0.86}$Ge$_{0.14}$ and 43 Å/min for Si$_{0.90}$Ge$_{0.10}$ at 550 °C, respectively. The maximum operation time for maintaining selective epitaxial growth of Si$_{0.90}$Ge$_{0.10}$ or Si$_{0.86}$Ge$_{0.14}$ layer (i.e., epitaxy on Si region only, but not on field oxide region) at 550 °C is above 90 min. Samples with epitaxial thickness of 50 nm and 100 nm were processed in order to study the effects of the epitaxial layer thickness on the device performance. For comparison, conventional Si MOS transistors (i.e., without any raised S/D layer) were also fabricated in the same run. To obtain higher degree of boron concentration in S/D region, a $10^{15}$ cm$^{-2}$, 20 KeV BF$_2$ implant was adopted, which is followed by a 900 °C, 30 s RTA for activation. Afterwards, a 500 nm TEOS was deposited, and a Ti/TiN/Al–Si–Cu/TiN 4-layer metal was deposited and patterned to complete contact metallization. Electrical characterizations at various temperatures ranging from 50 °C to 100 °C were performed with a HP4156 system, which was equipped with a thermal controller connected to the Cascade semi-auto probe station. Sheet resistance was extracted using bridge resistor test structures, while the contact resistance was measured by Kelvin cross-bridge structures.

III. RESULTS AND DISCUSSIONS

Fig. 1 compares the $I_D$–$V_G$ and transconductance ($g_m$) characteristics of MOS transistors with SiGe$_{0.14}$ and Si RSD samples. Both devices have the same epitaxial RSD thickness of 100 nm and the same effective channel length of 0.24 μm. By using Si$_{0.86}$Ge$_{0.14}$ RSD, $g_m$ and $I_D$ values (measured at $V_{DS} = -2.5$ V and $V_{GS} - V_T = -1.8$ V) of 127 mS/mm and 158.6 μA/μm, which are 19.02% and 16.11% higher than those of the counterpart device with Si RSD device, are obtained. These improvements are believed to be due to the lowering of the Schottky barrier height (SBH) in metal/p$^+\text{Si}_{1-x}\text{Ge}_x$ junction, which leads to the reduction of sheet resistance and specific contact resistivity [6]. The energy band gap ($E_g$) of Si$_{1-x}\text{Ge}_x$ is known to change from 1.12 to 0.66 eV with increasing Ge mole fraction [15]. For pseudomorphic p-Si$_{0.86}\text{Ge}_{0.14}$ layer, the SBH is expected to be lower than that of metal/p$^+$Si by 0.07 eV [16], thus effectively reduces the specific contact resistivity ($\rho_C$).

As shown in Fig. 2, the transconductance and relative contact resistivity measured by transmission line method (TLM) are plotted as a function of Ge mole fraction for devices with various channel lengths. The thickness of the epitaxial RSD layer is 50 nm. It can be seen that the effects of Ge on device performance become more dramatic when the devices are scaled down. For 0.24 μm, a 13% improvement in $g_m$ value could be obtained for SiGe$_{0.14}$ RSD, compared to the device with Si RSD.

With a thicker epitaxial RSD layer (e.g., 100 nm), shallower p$^+$ S/D junction could be obtained, especially for Si$_{1-x}\text{Ge}_x$ layer with higher Ge mole fraction [2], [17], [18]. Thus the susceptibility to punch-through and short channel effect could be alleviated, which is advantageous especially for sub-0.1 μm devices. Fig. 3 shows the drain-induced barrier lowering (DIBL) effects for PMOSFETs with various RSD structures.
without any RSD, improvement in DIBL is observed for the device with 100 nm Si$_{1-x}$Ge$_x$ RSD because the junction depth of the 100 nm Si$_{1-x}$Ge$_x$ RSD in the source and drain region would be as shallow as the depth of the extension region (<800 Å). In addition, the improvement in DIBL indeed increases with increasing Ge mole fraction. It is worthy to note that for device with a thick 100 nm Si$_{1-x}$Ge$_x$ RSD, the implant damage could be alleviated, because the damage region is located away from the p$^+$–n S/D junction. Thus no high temperature anneal (>900 °C) is necessary to anneal out defects caused by the implant damage, as is required in conventional Si PMOSFETs. The remarkable leakage current reduction at low $V_D$ level is indeed confirmed in Fig. 4 for devices with Si$_{1-x}$Ge$_x$ RSD, all devices with an effective channel length of 0.24 μm. On the other hand, there is essentially no difference in the gate induced drain leakage current (GIDL) that is measured at high $V_D$ bias. This is because the interface quality between gate and drain region for all samples remains essentially the same.

The effects of Si$_{1-x}$Ge$_x$ RSD on the low temperature operation of the transistors were also studied. Figs. 5 and 6 showed the subthreshold and transconductance characteristics measured at three different temperatures (i.e., 223, 298, and 373 K) for a conventional p-channel device (i.e., without any RSD) and the device with 100 nm Si$_{0.05}$Ge$_{0.95}$, respectively. Both the transconductance and the drain current increase with reducing temperature due to increased carrier mobility. At −50 °C, the transconductance value is 145 mS/mm and 169 mS/mm (measured at $V_D = -2.5$ V) for the conventional device and the device with Si$_{0.05}$Ge$_{0.95}$, respectively. Leakage current also achieves its lowest value at the lowest measurement temperature (i.e., −50 °C), because of reduced scattering rate and increased carrier mean free path. Generally, all aspects of $I$–$V$ characteristics approach their optimum conditions with reducing temperature. Threshold voltage $V_T$ decreases while temperature increases due to increased number of intrinsic carriers. Finally, the thermal behavior of the parasitic components in a transistor could also affect the output characteristics of the transistors. Standard $I_D$ versus $V_D$ characteristics for the conventional non-RSD device and the device with 100 nm Si$_{1-x}$Ge$_x$ RSD are shown in Fig. 7 for two operation temperatures, i.e., 223 K (−50 °C) and 298 K (25 °C). The channel width of the transistors is 100 μm. In the figure, solid and dotted lines denote the conventional device and the device with Si$_{0.05}$Ge$_{0.95}$ RSD operating at −50 °C (coarse lines) and 25 °C (thin lines), respectively. The improvements with reduced temperature are more dramatic for the device with Si$_{0.05}$Ge$_{0.95}$, as compared with the conventional device. The drain current (measured at $V_D = -2.5$ V, $V_G = V_T = -2.5$ V) are 286.5 μA/μm and 254.8 μA/μm for RSD Si$_{0.05}$Ge$_{0.95}$ and the conventional device at −50 °C. In order to confirm this phenomenon further, the saturation transconductance $g_{m}$ versus effective channel length $L_{eff}$ is plotted in Fig. 8. It reveals the superior room tempera-
ture and low-temperature performance in $g_m$ value for the device with Si$_{0.8}$Ge$_{0.14}$ RSD. For an effective channel length of 0.17 μm, the transconductance increases from 166 to 187 mS/mm as temperature changes from 25°C to −50°C for the device with Si$_{0.8}$Ge$_{0.14}$ RSD, which represents a 12.5% improvement in $g_m$. In contrast, the $g_m$ value changes from 135 to 146 under the same condition for the conventional device, which represents only 7.8% improvement for low-temperature operation.

To calculate the degree of improvements in transconductance, the normalized maximum linear $g_m$ value measured at −50°C with respect to the same parameter measured at 100°C is plotted as a function of the effective channel length in Fig. 9. The average ratio of enhancement is roughly 1.6 and 1.54 for the Si$_{0.8}$Ge$_{0.14}$ RSD device and the conventional device, respectively. For device operation in saturation mode, normalized drive current $I_{DS[−50{°}C]}/I_{DS[100{°}C]}$ (measured at $V_{DS}=−2.5$ V and $V_G=−2.5$ V) as a function of the effective channel length $L_{eff}$ is shown in Fig. 10. A remarkable improvement in the normalized drive current as temperature varied from 100°C to −50°C is again observed for devices with Si$_{1−x}$Ge$_x$ RSD, as compared with the conventional devices. It is worthy to note here that the normalized drive current $I_{DS[−50{°}C]}/I_{DS[100{°}C]}$ reduces with decreasing $L_{eff}$ for all devices. This trend is different from that of the normalized maximum linear $g_m$, which remains essentially constant with reducing $L_{eff}$. This is because when the device is operating in linear region (e.g., $V_{DS}=−0.1$ V), carrier velocity is under low electric field condition, mobility $\mu_T$ which is independent of channel length plays an important role in maximum linear $g_m$. As a result, a constant value in maximum linear $g_m$ versus $L_{eff}$ that is dependent only on temperature is observed for all devices. However, when the device is operating in saturation mode (e.g., $V_C=−2.5$ V, and $V_{DS}=−2.5$ V), a high electric field is generated along the channel and would become even higher as $L_{eff}$ decreases. Several factors, including velocity saturation, reduced carrier mobility caused by carrier scattering, and extrinsic component at high current drive would dominate and determine the $I_{DS[−50{°}C]}/I_{DS[100{°}C]}$ behavior, thus reduces the enhancement ratio as devices are scaled down.

In order to study further the temperature variations in intrinsic and extrinsic components of the transistors, sheet resistance $\rho_S$ and contact resistivity $\rho_C$ as a function of temperature were measured, and the results are shown in Figs. 11 and 12, respectively. Generally, sheet resistance in source and drain region, extension layer, and channel resistance decreases with reducing temperature due to enhanced mobility. On the contrary, specific contact resistivity increases with reducing temperature because less number of carriers would be able to overcome the metal/semiconductor energy barrier (SBH) by thermionic emission. This is especially true for the conventional device with higher energy barrier. The superior low-temperature behavior of the Si$_{1−x}$Ge$_x$ RSD device can be elucidated by the basic MOSFET model [19]. A MOSFET can always be broken down into an intrinsic MOS device and extrinsic source and drain resistive components. The entire extrinsic transconductance is

$$g_m = \frac{1}{g_{m0} + R_{Source}}$$

where $g_{m0}$ is the transconductance of the intrinsic device, $R_{Source}$ denotes the parasitic resistance including sheet resistance, contact resistance, and extension resistance, etc. The measured contact resistance values for a $2 \times 2$ μm contact are 45.82, 3.17, and 1.94 Ω, while the sheet resistance values at 298 K are 132.5, 84.6, and 96.48 Ω/□ for conventional, Si$_{0.21}$Ge$_{0.09}$ RSD, Si$_{0.8}$Ge$_{0.14}$ RSD, respectively. Since the contact resistance is relatively small, the entire $R_{Source}$ is

Fig. 8. Saturated transconductance $g_m$ versus effective gate length measured at various temperatures for conventional and Si$_{0.8}$Ge$_{0.14}$ RSD devices.

Fig. 9. Normalized $g_m[−50{°}C]/g_m[100{°}C]$ versus effective channel length for conventional and Si$_{0.8}$Ge$_{0.14}$ RSD devices.

Fig. 10. Normalized $I_{DS[−50{°}C]}/I_{DS[100{°}C]}$ versus effective channel length for conventional and Si$_{0.8}$Ge$_{0.14}$ RSD, and Si$_{0.8}$Ge$_{0.09}$ RSD devices.
temperature operation, which can be explained by the higher temperature sensitivity of the resistance of Si$_{1-x}$Ge$_x$ RSD.

These performance improvements thus make Si$_{1-x}$Ge$_x$ RSD structure very attractive for future sub-0.1 µm p-channel MOS transistors.

ACKNOWLEDGMENT

The authors would like to thank Dr. H. C. Lin for experimental assistance.

REFERENCES


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He has devoted himself to education and academic research for more than 40 years. He has contributed profoundly to the areas of microelectronics and optoelectronics, including the invention of the method of low-pressure-MOCVD-using tri-ethyl-gallium to fabricate LED, laser, and microwave transistors, Zn-incorporation of SiO2 for stabilization of power devices, and nitridation of SiO2 for ULSIs, etc. From 1962 to 1963, he fulfilled his military service by establishing at NCTU Taiwan’s first experimental TV transmitter that formed the founding structure of today’s CTS. In 1963, he joined NCTU to serve as an instructor establishing a high vacuum laboratory. In 1964, he and his colleague established the semiconductor research center (SRC) at NCTU with a very up-to-date, albeit homemade, facility for silicon device processing, where they made the nation’s first Si Planar transistor in April 1965, and subsequently the first IC in August 1966. In 1968, he published Taiwan’s first-ever semiconductor paper in the international journal Solid State Electronics. In 1969, he became a Full Professor, teaching solid state physics, quantum mechanics, semiconductor devices and technologies. From 1977 through 1987, he single-handedly established a strong electrical engineering and computer science program at NCKU where GaAs, α-Si, poly-Si researches were established in Taiwan for the first time. Since 1987 he served consecutively as Dean of Research (1987–1990), Dean of Engineering (1990–1994), and Dean of Electrical Engineering and Computer Science (1994–1995). Simultaneously he was serving as the founding president of National Nano Device Laboratories (NDL) from 1990 through 1997. In 1997, he became Director of the Microelectronics and Information System Research Center (MIRC), NCTU (1997–1998). Many of his former students have since become founders of the most influential Hi-Tech enterprises in Taiwan, namely UMC, TSMC, Winbond, MOSEL, Acer, Leo, etc. In August 1, 1998, he was appointed as the President of NCTU. As the National-Chair-Professor and President of NCTU, his vision is to lead the university for excellence in engineering, humanity, art, science, management and bio-technology. To strive forward to world class multidisciplinary university is the main goal to which he and his colleagues have committed.

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