The Copper Contamination Effect of Al₂O₃ Gate Dielectric on Si

C. C. Liao, C. F. Cheng,² D. S. Yu, and Albert Chin

Department of Electronics Engineering, National Chiao Tung University, Nano Science and Technology Center, University System of Taiwan, Hsinchu, Taiwan

We have studied the Cu contamination effect on 4.2 nm thick Al₂O₃ metal-oxide semiconductor (MOS) capacitors with an equivalent-oxide thickness (EOT) of 1.9 nm. In contrast to the large degradation of gate oxide integrity of control 3.0 nm SiO₂ MOS devices, the Cu contamination effect was studied by contacting the front metal-oxide semiconductor (MOS) devices with 3.0 nm thermal SiO₂ are also added for comparison. The 1.9 nm EOT Al₂O₃ gate dielectric MOS capacitors contaminated by Cu, the 1.9 nm EOT Al₂O₃ MOS devices have good Cu contamination resistance with only small degradation of gate dielectric leakage current, charge-to-breakdown, and stress-induced leakage current. This strong Cu contamination resistance is similar to stoichiometric (with high nitrogen content), but the Al₂O₃ gate dielectric has the advantage of higher κ value and lower gate dielectric leakage current.

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To reduce the circuit’s RC delay from back-end metal lines and parasitic capacitors, Cu and low-κ dielectric are required. However, Cu diffusion into low-κ and front-end metal-oxide semiconductor field effect transistors (MOSFETs) is an important issue.¹ ¹² The Cu contamination from back-end Cu interconnects or the back-side wafer surface contaminated by Cu accumulates at the Si/SiO₂ interface or reacts with Si to form silicide. The precipitate Cu at the oxide interface increases the subthreshold swing of MOSFETs,² ³ shifts the threshold voltage, and degrades the gate leakage current.¹ ¹² The Cu silicide also increases the unwanted leakage current in the source-drain junction. To reduce Cu diffusion during back-end thermal cycling, a barrier metal under Cu and thick SiN between each intermetal layer (IML) dielectric are usually added. However, the added SiN of typically 50 nm has a χ value of 7.5 and degrades the total κ of combined IML dielectric and SiN. The increasing effective κ is unfavorable because it increases the circuit’s back-end resistance-capacitance (RC) delay. In this paper, we have studied the Cu contamination effect in high-κ Al₂O₃ gate dielectric with small equivalent-oxide thickness (EOT) of 1.9 nm, where the high-κ gate dielectric is important for continuously scaling down the nanometer-scale MOSFET. In contrast to the large degradation of gate oxide integrity in 3.0 nm thermal SiO₂, the smaller 1.9 nm EOT Al₂O₃ gate dielectric shows much better resistance to Cu contamination-related degradation on gate dielectric leakage current, charge-to-breakdown (Qbd), and stress-induced leakage current (SILC). Therefore, the high-κ gate dielectric with Al₂O₃ ternary compound such as HfAlO or LaAlO₃ should have this additional advantage besides the high-κ value. This is the first study of Cu diffusion in high-κ Al₂O₃.

Experimental

Standard 4 in., p-type Si(100) wafers with a typical resistivity of ~10 Ohm-cm were used in this study. After standard cleaning, the device active region was formed by thick field oxide and patterning. Then the ~4.2 nm Al₂O₃ was formed by physical-vapor deposition from an Al₂O₃ sputter source, oxidation at 400°C under O₂ ambient for 5 min, and annealed at N₂ ambient for 25 min. From the capacitance-voltage (C-V) measurement, a κ value of 8.5 and EOT of 1.9 nm were obtained. Then the gate electrode was formed by depositing a 300 nm thick aluminum by thermal evaporation and patterning, where the fabricated area of MOS capacitors is 100 × 100 μm. The Cu contamination to the Al₂O₃ gate-oxide semiconductor (MOS) devices was introduced by contacting the front side of devices into a Cu(NO₃)₂ solution with 10 ppb or 10 ppm concentration for 1 min followed by driving-in at 400°C N₂ annealing.

The existence of Cu within gate SiO₂ by this contamination process was confirmed by secondary ion mass spectroscopy (SIMS) measurements reported previously,¹³ where strong Cu accumulation is observed in both poly-Si and SiO₂. A more detailed Cu contamination process and discussion of degradation on gate dielectric integrity of SiO₂ and SiON can be found in our previous publications.¹ ¹² The Cu contamination effect was studied by current-density and voltage (J-V) measurements in high-κ Al₂O₃ gate dielectric MOS capacitors.

Results and Discussion

Figure 1 shows the J-(VＧ, Vfb) characteristics of Al₂O₃ gate capacitors with ~4.2 nm physical thickness (1.9 nm EOT), where the Vfb is the flatband voltage obtained from the C-V measurement and quantum mechanical calculation. The Vfb of ~0.7 and ~0.85 V are obtained for Al₂O₃ and SiO₂ gate dielectric capacitors, respectively. There is no significant Vfb change after Cu contamination. This suggests that the Cu may behave as a neutral trap in the gate dielectric, consistent with our previous report.¹² For comparison, the J-(VＧ, Vfb) characteristics of a 3.0 nm thick SiO₂ MOS device were also plotted. For samples without Cu contamination, the 1.9 nm EOT Al₂O₃ gate capacitor has a one order of magnitude lower leakage current than 3.0 nm SiO₂, which is the fundamental advan-

Figure 1. The J-(VＧ, Vfb) characteristics of MOS capacitors with 4.2 nm Al₂O₃ gate dielectric (1.9 nm EOT) with or without Cu contamination. The MOS devices with 3.0 nm thermal SiO₂ are also added for comparison. The devices were contaminated by 10 ppb or 10 ppm Cu.
The Cu contamination in 3.0 nm SiO₂ control devices have a significant effect on gate dielectric leakage current, which was increased by ca. two orders of magnitude. The 10 ppb and 10 ppm Cu-contaminated SiO₂ control devices show almost identical leakage current before breakdown voltage (V_{BD}), although the V_{BD} is lower in 10 ppm contaminated devices than the 10 ppb case. Such effect was previously attributed to the Cu trap energy state inside the SiO₂ dielectric; the leakage current shows an exponential relation with the trap energy in direct tunneling regime with less concentration dependence. In contrast to the large increasing leakage current in SiO₂ MOS capacitors contaminated by Cu, negligible leakage current increase in Al₂O₃ MOS capacitors is measured with high 10 ppm Cu contamination. The reason the Cu contamination has little effect on the Al₂O₃ gate dielectric may be due to the strong diffusion barrier property similar to Si₃N₄, where the Al₂O₃ can even be used as the diffusion barrier for a small H₂ molecule.¹⁷

Figure 2a-c further compares the cumulative leakage current distributions of the 4.2 nm Al₂O₃ (1.9 nm EOT), 3.0 nm SiO₂, and 3.6 nm SiON with 23% N content (3.0 nm EOT) gate dielectrics with or without Cu contamination.
In sharp contrast, only slightly increasing leakage current at lowest 0.5 V bias can be observed in the 4.2 nm Al₂O₃ (1.9 nm EOT). This increasing leakage current in the pretunneling region at low voltage is also previously observed in thick 5.0 nm SiO₂ and oxynitride with 16% N content, which is attributed to the trap-assisted tunneling originated by neutral traps formed by Cu inside the oxide matrix. It is noticed that although the degradation of pre-tunneling leakage current is negligible for the 3.6 nm oxynitride with 23% N, the Al₂O₃ still has strong advantage of much smaller EOT of only 1.9 nm than the 3.0 nm EOT oxynitride. In addition, the k-value of 8.5 for Al₂O₃ is also higher than the 4.7 k-value for 23% N oxynitride, which is important for gate dielectric application in nanometer-scale MOSFETs.

Figure 4a shows the comparison of QBD distribution of 4.2 nm Al₂O₃ gate dielectric (1.9 nm EOT) and 3.0 nm SiO₂. The applied stress condition is at −3.3 V for 10,000 s. 10 ppm has only small effects on QBD distribution of the 1.9 nm EOT Al₂O₃ gate dielectric and is free from the tail QBD distribution devices. This result is also consistent with the tight gate current distribution shown in Fig. 2a. It is noticed that the QBD value decreases rapidly with increasing stress voltage, and the mean QBD of 0.4 C/cm² for 4.2 nm Al₂O₃ gate dielectric, biased at a large voltage of 5.8 V, is also comparable to SiO₂ within the same order. This suggests the excellent quality of high-k Al₂O₃ gate dielectric. Figure 3b further shows the time-to-breakdown (tBD) plot stressed at −4 V at 150°C. The larger tBD decrease of Cu-contaminated SiO₂ than that of Al₂O₃ is due to the larger increase of leakage current in SiO₂ after contamination shown in Fig. 1.

The SILC is another important factor for gate dielectric reliability evaluation. Figure 4a and b shows the comparison of the stress effect on J-V characteristics for MOS capacitors with 4.2 nm Al₂O₃ gate dielectric and 3.0 nm SiO₂ MOS capacitors.
improved gate leakage current. Among all the Al$_2$O$_3$ and SiO$_2$ MOS devices with or without Cu contamination, the control 3.0 nm SiO$_2$ MOS capacitor has the smallest current change and better than the 4.2 nm Al$_2$O$_3$ MOS device under the same stress condition. This is due to the robustness of thermal SiO$_2$ where larger bulk oxide and interface defects are usually found in high-$k$ dielectric such as Al$_2$O$_3$. The amount of these weak defects increases under charge injection during constant voltage stress, which causes higher leakage current in MOS capacitors.

To further analyze the SILC effect, we have plotted the current change ($J_	ext{stressed}/J_0$) as a function of bias voltage in Fig. 5, which is more sensitive than the $J_	ext{stressed}$-$V$ plot shown in Fig. 4. For the uncontaminated Al$_2$O$_3$ and SiO$_2$ MOS devices shown in Fig. 5a and b, respectively, the Al$_2$O$_3$ dielectric capacitor has higher SILC current than the SiO$_2$ devices, even though the dielectric thickness (4.2 nm) for Al$_2$O$_3$ is thicker than the SiO$_2$ (3.0 nm). This is due to the higher bulk and interface defects in high-$k$ Al$_2$O$_3$ gate dielectric than thermal SiO$_2$. However, the SILC of $\Delta J/J_0$ increases rapidly in the SiO$_2$ devices even under the smallest Cu contamination of 10 ppb. The increasing SILC with Cu contamination is previously attributed to the formation of neutral traps inside the oxide and interface. 12 In contrast, the $\Delta J/J_0$ only increases slightly at 10 ppb Cu contamination and the amount of increase at 10 ppm Cu is still less than the SiO$_2$ case. The smaller amount of Cu-contamination-generated SILC in Al$_2$O$_3$ gate dielectric suggests the good diffusion barrier property and is also consistent with the smaller degradation on dielectric leakage current and $Q_{BD}$ shown in Fig. 1 and 3.

**Conclusion**

We have studied the Cu contamination effects on gate dielectric integrity of 4.2 nm Al$_2$O$_3$ dielectric. By comparing with the control 3.0 nm SiO$_2$ MOS capacitors contaminated by Cu, much smaller degradation of gate dielectric leakage current, $Q_{BD}$ and SILC is found in 1.9 nm EOT Al$_2$O$_3$ MOS devices. The much better resistance of Cu contamination in ultrathin 1.9 nm EOT Al$_2$O$_3$ MOS capacitor is the strong advantage for high-$k$ Al$_2$O$_3$ gate dielectric.

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