A CF$_4$ plasma treatment on solid-phase-crystallized (SPC) poly-Si thin-film transistors (TFTs) has been demonstrated. Using this technique, fluorine atoms can be introduced into the poly-Si film to passivate the defects, and hence, the SPC poly-Si TFTs can be significantly improved. The fluorinated SPC poly-Si TFTs exhibit a good subthreshold slope, low threshold voltage, and high field effect mobility. Moreover, the fluorinated SPC poly-Si TFTs also exhibit an improved hot-carrier-stress immunity, which is due to the strong Si-F bonds formed in the poly-Si channel region.

Experimental

The schematic diagram of the fabrication process is illustrated in Fig. 1. First, a 100-nm-thick amorphous silicon layer was deposited on a thermally oxidized Si wafer by dissociation of SiH$_4$ gas in a low-pressure chemical vapor deposition (LPCVD) system at 550°C. Subsequently, solid phase crystallization (SPC) was performed at 600°C for 24 h in N$_2$ ambient for the phase transformation from amorphous to polycrystalline silicon. Individual active regions were then patterned and defined. After standard RCA cleaning, samples were subjected to the CF$_4$ plasma treatment conducted in a plasma-enhanced chemical vapor deposition (PECVD) system at 350°C for 15 s, under a pressure of 200 mTorr and a power of 5 W. A 50-nm-thick tetraethoxysilicate (TEOS) oxide was deposited to serve as the gate insulator and a 200-nm-thick poly-Si film was deposited and patterned for the gate electrode. A self-aligned phosphorus ion implantation was performed with the dosage and energy of 5 × 10$^{15}$ cm$^{-2}$ and 40 keV, respectively. The dopant activation was performed at 600°C furnace annealing at N$_2$ ambient for 24 h, followed by a deposition of the passivation layer and a definition of contact holes. Finally, a 500-nm-thick Al electrode was deposited and patterned. The control samples were prepared without the fluorinating process. To concentrate on revealing the fluorine passivating effects of the CF$_4$ plasma treatment, none of the additional hydrogenation process was performed on the control samples. The electrical and reliability characteristics were performed using an HP 4156B.

Results and Discussion

Figure 2 shows the transfer characteristics ($I_D - V_{GS}$) for the control and fluorinated poly-Si TFTs. The measurements were performed at two different drain voltages of $V_{DS}$ = 0.1 and 5 V. The parameters of the devices, including the threshold voltage ($V_{th}$) and subthreshold swing (S.S.), maximum on-current ($I_{on}$) and the minimum off-current ($I_{off}$), were measured at $V_{DS} = 5$ V. The threshold voltage was defined as the gate voltage required to achieve a normalized drain current of $I_D = (W/L) \times 100$ nA. The extracted device parameters are listed in Table I.

Accordingly, the performance of the fluorinated poly-Si TFT is significantly improved. The threshold voltage and subthreshold swing of the fluorinated poly-Si TFT were found to be 8.3 and 1.73 V/dec, which are superior to that of the control one (12 and 2.06 V/dec, respectively). It is known that $V_{th}$ and S.S. are strongly influenced by the deep trap states, associated with the dangling bonds, which have energy states near the middle of the silicon bandgap. Therefore, using CF$_4$ plasma treatment can effectively terminate the dangling bonds in the poly-Si and SiO$_2$/poly-Si interface. In addition, the maximum on-current ($I_{on}$) and on/off current ratio of the fluorinated TFT are also better than that of the control TFT.

The minimum off-current ($I_{off}$) of the fluorinated device was nearly unsuppressed, which is consistent with the previous reports by Chern et al. and Kim et al. However, while the applied gate voltage was toward more negative ($V_{GS} < -2$ V), the fluorinated poly-Si TFT showed a smaller leakage current compared with that of the control TFT. As is well known, under a high electric field, the
leakage current in the poly-Si TFT mainly comes from the trap-assisted band-to-band tunneling near the drain edge. This observation suggests that there must be fewer trap states for the fluorinated poly-Si TFT, and thus the leakage current under a high electric field is reduced.

Figure 2 also shows field effect mobility vs the gate voltage of control and fluorinated poly-Si TFTs. The field effect mobility was calculated from the value of transconductance at $V_{DS} = 0.1$ V. As is seen, the maximum field effect mobility of the fluorinated poly-Si TFT is higher than that of the control TFT. The fluorinated poly-Si TFT shows approximately 28% enhancement in the maximum field effect mobility. Note that the field effect mobility is significantly affected by the tail states near the band edge, which resulted from the strain bonds in poly-Si and SiO$_2$/poly-Si interfaces. This feature implies that the CF$_4$ plasma treatment cannot only terminate the dangling bonds, but also relieve the strain bonds. Based on these results, a schematic cross-sectional view of the SiO$_2$/poly-Si interface is illustrated in Fig. 3. It is suggested that strong Si-F bonds replace the dangling and strain bonds for the fluorinated poly-Si films, and thus the performance of the device is greatly improved.

The grain boundary trap state densities ($Q_T$) of the conventional and fluorinated poly-Si TFTs were estimated by the Levison and Proano method.$^{16,17}$ Figure 4 exhibits the $\ln(\mu/\mu_0)$ vs $1/(V_{GS} - V_{FB})^2$ curves at low $V_{GS}$ and high $V_{GS}$. $Q_T$ was extracted from the slopes of these curves. Fluorinated poly-Si TFT exhibits a $Q_T$ of $1.32 \times 10^{13}$ cm$^{-2}$, whereas the control TFT has $1.67 \times 10^{13}$ cm$^{-2}$. This result implies that the CF$_4$ plasma treatment passivates the grain boundary trap states in the poly-Si film. To further study the fluorine passivation effect near the interface, the effective interface trap states densities ($N_t$) near the SiO$_2$/poly-Si interface were also calculated. From the S.S., by neglecting the depletion capacitance, $N_t$ can be expressed as:

$$N_t = \left[\frac{(S.S./\ln 10)(q/kT) - 1}{C_{ox}/q}\right]$$

where $C_{ox}$ is the capacitance of the gate oxide. The $N_t$ values of the control TFT and the fluorinated TFT are 1.45 and 1.21 $\times 10^{13}$ cm$^{-2}$, respectively. The $N_t$ values reflect trap states near the SiO$_2$/poly-Si interface. Therefore, these results figure that trap states in both grain boundaries and the SiO$_2$/poly-Si interface were reduced by using CF$_4$ plasma treatment, which results in great improvement in device performance.
Figure 5 shows the output characteristics ($I_D$ − $V_{DS}$) of the fluorinated and control poly-Si TFTs. As is seen, the driving current increases significantly for the fluorinated poly-Si TFT. This is due to the higher mobility and smaller threshold voltage of the fluorinated poly-Si TFT compared with the control TFT. The driving current increased 130, 84, and 55% at $V_{DS} = 20$ V with $V_{GS} = 10$, 15, and 25 V, respectively. Figure 6 shows the secondary ion mass spectroscopy (SIMS) profiles of the control and fluorinated poly-Si films. The SIMS profiles show that lots of fluorine atoms could be introduced into the poly-Si layer by using CF$_4$ plasma treatment, but not carbon atoms. The SIMS analysis also shows a notably high concentration of fluorine atoms piling up near the SiO$_2$/poly-Si interface, instead of in the deep poly-Si layer. These piled-up fluorine atoms can provide a more effective passivation of trap states, because the quality of the SiO$_2$/poly-Si interface is the main issue for carrier transport.

Figure 7 exhibits activation energy ($E_a$) vs gate voltage for the control and fluorinated poly-Si TFTs at $V_{DS} = 1$ V. In the off-region (low $V_{GS}$), the value of $E_a$ reflects the required energy for carriers to leak by means of trap states, whereas in the on-region (high $V_{GS}$), the value of $E_a$ reflects the carrier transport barrier caused by the trap states within the poly-Si channel. Compared with the control TFT, the extracted $E_a$ of the fluorinated poly-Si TFT decreases in the on-region and increases in the off-region. That is to say, for fluorinated poly-Si TFT, fluorine atoms can passivate the trap states and hence reduce the barrier height for the carrier’s transport when the device is turned on. Fewer trap states resulted in the increase of $E_a$ in the off-region and thus, trap-assisted leakage current is suppressed after the fluorinating process. Moreover, in the subthreshold region, a steeper profile can be found for the fluorinated TFT, which proves that the interface quality of the fluorinated TFT was better than that of the control TFT.
was suppressed for the fluorinated sample. As a result, device reliability was greatly improved for the fluorinated poly-Si TFT.

Conclusion

We reported a novel fluorinating technique of poly-Si TFTs by employing CF₄ plasma treatment. Using this technique, significant improvements in the performance of fluorinated poly-Si TFTs have been demonstrated. A steeper subthreshold slope, smaller threshold voltage, higher carrier mobility, and better on/off current ratio can be obtained due to the reduction of trap states in the poly-Si and the SiO₂/poly-Si interface. Moreover, the CF₄ fluorinating process also improves hot-carrier immunity. It is concluded that the CF₄ fluorination technique can provide a simple, effective, and process-compatible method to introduce fluorine atoms into poly-Si film to fabricate high-performance as well as high-reliability poly-Si TFTs.

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Figure 8. On-current variation as a function of stress time under a hot-carrier stress of the control and fluorinated poly-Si TFTs.