Effects of layer sequence and postdeposition annealing temperature on performance of La$_2$O$_3$ and HfO$_2$ multilayer composite oxides on In$_{0.53}$Ga$_{0.47}$As for MOS capacitor application

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In this paper, we report on high-k composite oxides that are formed by depositing multiple layers of HfO2 and La2O3 on In0.53Ga0.47As for MOS device application. Both multilayer HfO2 (0.8 nm)/La2O3 (0.8 nm)/In0.53Ga0.47As and La2O3 (0.8 nm)/HfO2 (0.8 nm)/In0.53Ga0.47As MOS structures were investigated. The effects of oxide thickness and postdeposition annealing (PDA) temperature on the interface properties of the composite oxide MOS capacitors were studied. It was found that a low CET of 1.41 nm at 1 kHz was achieved using three-layer composite oxides. On the other hand, a small frequency dispersion of 2.8% and an excellent oxide of 7.0 \frac{\text{cm}^2}{\text{V}\cdot\text{s}} at 1 \text{kHz} was obtained. © 2014 The Japan Society of Applied Physics

Figure 1 shows the X-ray photoelectron spectroscopy (XPS) spectra of the HfO2 (0.8 nm)/La2O3 (0.8 nm)/n-In0.53Ga0.47As and La2O3 (0.8 nm)/HfO2 (0.8 nm)/n-In0.53Ga0.47As composite oxide structures annealed at 400, 500, and 550 °C in N2 for 5 min. The As 3d, Ga 2p, In 3d, and O 1s XPS spectra of the samples with different PDA temperatures were analyzed to determine the film compositions and interface properties. In general, with increasing PDA temperature, more interactions between oxides and semiconductors occur, and the number of As–O bonds is reduced owing to the high-temperature annealing, as indicated by As 3d in Fig. 1. When the PDA temperature was increased to 500 °C, the amounts of As-, Ga-, and In-related oxides decreased for both composite oxide structures. The amount of La2O3 increased for the La2O3/HfO2/n-In0.53Ga0.47As structure, as indicated by the XPS O 1s peak in Fig. 1. The slight reduction of the native oxides could be explained by the conversion of As–O, Ga–O, and In–O bonds to InAs, GaAs, and La2O3 during thermal annealing for the La2O3/HfO2/n-In0.53Ga0.47As structure. However, the amount of La2O3 that diffused into InGaAs increased with temperature for the HfO2/La2O3/n-In0.53Ga0.47As structure. The 500 °C annealing not only converted the As–O, Ga–O, and In–O bonds to InAs and GaAs bonds but also resulted in the increase in the amount of La2O3 diffusing into InGaAs for the HfO2/La2O3/n-In0.53Ga0.47As structure. Furthermore, the amounts of As-, Ga-, and In-related oxides increased significantly for both composite oxide structures when the PDA temperature was increased to 550 °C, as indicated by the As 3d, Ga 2p, and In 3d spectra in Fig. 1. This indicates that at the PDA temperature of 550 °C, the diffusions of As, Ga, and In into the oxide layers were quite significant for both composite oxide structures.

Figure 2 shows the comparison of capacitance–voltage (C–V) curves at 1 MHz for the five layers of HfO2 (0.8 nm)/La2O3 (0.8 nm) and the five layers of La2O3 (0.8 nm)/HfO2 (0.8 nm) composite oxides on n-In0.53Ga0.47As MOS capacitors, and the HfO2 (8 nm)/n-In0.53Ga0.47As MOS capacitors, and the HfO2 (8 nm)/n-In0.53Ga0.47As MOS capacitors.
capacitor. The electrical characteristics of the composite oxide MOS capacitor were markedly improved when the devices were annealed at the PDA temperature of 500 °C in N2 for 5 min. The dielectric constants of 15.2 and 14.8 were estimated for the five layers of the La2O3 (0.8 nm)/HfO2 (0.8 nm) and HfO2 (0.8 nm)/La2O3 (0.8 nm) composite oxides on n-In0.53Ga0.47As MOS capacitors, respectively.

Some reports show that the semiconductor elements will diffuse into the oxide after annealing, resulting in the decrease in the oxide dielectric constant and the increase in the device capacitance equivalent thickness (CET). In this case, CET = \( \frac{\varepsilon_0 \varepsilon_{SiO2}}{C(\text{accum.}\@ f = 1 \text{kHz})} \), where \( C(\text{accum.}\@ f = 1 \text{kHz}) \) is the capacitance of the accumulation region at frequency = 1 kHz, \( \varepsilon_0 \) is the vacuum permittivity, and \( \varepsilon_{SiO2} \) is relative permittivity of SiO2. A CET of 2.2 nm at 1 kHz with a low interface trap density \( (D_{it}) \) of \( 7.0 \times 10^{11} \) cm\(^{-2}\)eV\(^{-1}\) was achieved, as estimated by the conductance method for the La2O3/HfO2/n-In0.53Ga0.47As capacitor, as shown in Fig. 3(a). A higher \( D_{it} \) and a lower CET were obtained for the HfO2 (0.8 nm)/La2O3 (0.8 nm)/n-In0.53Ga0.47As device owing to the strong interaction between La2O3 and n-In0.53Ga0.47As. When the PDA temperature was increased, the interaction between the oxide and the semiconductor increased. The \( G_p/wqA \) vs frequency plot and \( D_{it} \) vs energy plot for the 5 layers of La2O3 (0.8 nm)/HfO2 (0.8 nm) and HfO2 (0.8 nm) on n-In0.53Ga0.47As MOS capacitors with PDA at 500 °C are shown in Figs. 4(a) and 4(b), respectively. From Fig. 4(b), the low \( D_{it} \) of \( 7.0 \times 10^{11} \) to \( 1.0 \times 10^{12} \) cm\(^{-2}\)eV\(^{-1}\) in the energy range of 0.47 to 0.44 eV above the In0.53Ga0.47As valence band maximum was obtained for the La2O3 (0.8 nm)/HfO2 (0.8 nm)/n-In0.53Ga0.47As device owing to the strong interaction between La2O3 and n-In0.53Ga0.47As. When the PDA temperature was increased to 550 °C, the capacitance decreased from 1.46 (500 °C) to 1.39 µF/cm\(^2\) (550 °C) and 1.44 (500 °C) to 1.20 µF/cm\(^2\) (550 °C) for the La2O3/HfO2/n-In0.53Ga0.47As structure and HfO2/La2O3/n-In0.53Ga0.47As structure, respectively. The larger capacitance decrease, particularly for the HfO2 (0.8 nm)/La2O3 (0.8 nm)/n-In0.53Ga0.47As capacitor, was due to the strong interdiffusion between La2O3 and InGaAs after high-temperature annealing. The \( C-V \) characteristics of the composite oxide capacitors with PDA temperatures of 400, 500, and 550 °C and different oxide thicknesses are compared in Table I.
Furthermore, the device performance was further improved by forming gas (5% H₂ + 95% N₂) annealing. Figure 5 shows the $C-V$ characteristics of the 5 layers of La₂O₃ (0.8 nm)/HfO₂ (0.8 nm) and the 5 layers of La₂O₃ (0.8 nm)/HfO₂ (0.8 nm) on n-In₀.₅₃Ga₀.₄₇As MOS capacitors with PDA at 500 °C in forming gas for 5 min. Frequency dispersion was improved owing to H₂ treatment, especially for the La₂O₃/HfO₂/n-In₀.₅₃Ga₀.₄₇As structure. The frequency dispersions were reduced from 3.5 to 2.9% and 2.8 to 2.6% for the La₂O₃/HfO₂/n-In₀.₅₃Ga₀.₄₇As structure and HfO₂/La₂O₃/n-In₀.₅₃Ga₀.₄₇As structure, respectively. However, the capacitances of both devices decreased after forming.

Table I. Comparison of $C-V$ characteristics of HfO₂ (8 nm)/n-In₀.₅₃Ga₀.₄₇As, La₂O₃ (0.8 nm)/HfO₂ (0.8 nm)/n-In₀.₅₃Ga₀.₄₇As and HfO₂ (0.8 nm)/La₂O₃ (0.8 nm)/n-In₀.₅₃Ga₀.₄₇As MOS capacitors.

<table>
<thead>
<tr>
<th>Device oxide structure</th>
<th>CET at 1 kHz (nm)</th>
<th>Accumulation capacitance (µF/cm²) at 1 kHz</th>
<th>Frequency dispersion (%)</th>
<th>Dit (10¹² cm⁻² eV⁻¹) at 1 kHz at 1 MHz</th>
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<tr>
<td>8 nm HfO₂ PDA at 500 °C in N₂</td>
<td>2.71</td>
<td>1.30</td>
<td>1.07</td>
<td>5.1</td>
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<tr>
<td>(La₂O₃/HfO₂) × 5 PDA at (°C)</td>
<td>500</td>
<td>N₂</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>500</td>
<td>Forming gas</td>
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<td>1.51</td>
<td>1.42</td>
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<tr>
<td>550</td>
<td>N₂</td>
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<td>1.41</td>
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<td>550</td>
<td>N₂</td>
<td>2.52</td>
<td>1.40</td>
<td>1.20</td>
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</tbody>
</table>

Fig. 3. $C-V$ characteristics of 5 layers of (a) La₂O₃ (0.8 nm)/HfO₂ (0.8 nm) and (b) HfO₂ (0.8 nm)/La₂O₃ (0.8 nm) on n-In₀.₅₃Ga₀.₄₇As MOS capacitors with PDA at 500 °C in N₂ gas for 5 min.

Fig. 4. (a) $G_p/wqA$ (A: 1.33 × 10⁻⁴ cm²) vs frequency curves at different gate biases and (b) Dit vs energy curves after 500 °C PDA for 5 layers of La₂O₃ (0.8 nm)/HfO₂ (0.8 nm) and HfO₂ (0.8 nm)/La₂O₃ (0.8 nm) on n-In₀.₅₃Ga₀.₄₇As MOS devices.
In summary, high-k composite dielectrics composed of La$_2$O$_3$ and HfO$_2$ layers on n-In$_{0.53}$Ga$_{0.47}$As for MOS capacitor application are investigated. Overall, the La$_2$O$_3$/HfO$_2$ structure on the n-In$_{0.53}$Ga$_{0.47}$As MOS capacitor demonstrates better performance than the HfO$_2$/La$_2$O$_3$ structure on the n-In$_{0.53}$Ga$_{0.47}$As MOS capacitor after thermal treatment owing to the interaction between the composite oxides and InGaAs materials. A low CET of 1.41 nm at 1 kHz for 3 layers, a small frequency dispersion of 2.6%, and an excellent $D_k$ of $7.0 \times 10^{11}$ cm$^{-2}$·eV$^{-1}$ can be achieved using multiple layers of La$_2$O$_3$ (0.8 nm) and HfO$_2$ (0.8 nm) on In$_{0.53}$Ga$_{0.47}$As MOS capacitors with PDA at 500°C.

Acknowledgment
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Fig. 5. $C$–$V$ characteristics of the five layers of (a) La$_2$O$_3$ (0.8 nm)/HfO$_2$ (0.8 nm) and (b) HfO$_2$ (0.8 nm)/La$_2$O$_3$ (0.8 nm) on n-In$_{0.53}$Ga$_{0.47}$As MOS capacitors with PDA at 500°C in forming gas for 5 min.

Fig. 6. $C$–$V$ characteristics of three layers of La$_2$O$_3$ (0.8 nm)/HfO$_2$ (0.8 nm) on n-In$_{0.53}$Ga$_{0.47}$As MOS capacitors with PDA at 500°C in nitrogen gas for 5 min.

gas annealing. The device CET was improved for the 3 and 4 layers of the La$_2$O$_3$ (0.8 nm)/HfO$_2$ (0.8 nm) structure on the n-In$_{0.53}$Ga$_{0.47}$As device after PDA at 500°C for 5 min in N$_2$ atmosphere. The $C$–$V$ curves for the 3-layer device are shown in Fig. 6; for the composite oxide with 3 and 4 layers of the La$_2$O$_3$ (0.8 nm)/HfO$_2$ (0.8 nm) structure, the CETs were reduced to 1.77 and 1.41 nm, respectively, after 500°C annealing, as measured at 1 kHz.