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Nickel Nanocrystals Embedded in Metal–Alumina–Nitride–Oxide–Silicon Type Low-Temperature Polycrystalline-Silicon Thin-Film Transistor for Low-Voltage Nonvolatile Memory Application

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In this work, a nickel nanocrystal (Ni-NC) assisted metal–alumina–nitride–oxide–silicon (MANOS) thin-film transistor (TFT) nonvolatile memory (NVM) was fabricated by a standard low temperature polycrystalline silicon (LTPS) TFT process. The size range and density of Ni-NCs were approximately 5–13 nm and 5 × 10¹¹ cm⁻², respectively. The programming/erasing (P/E) voltages were decreased down to −10 and +8 V, respectively, by the Fowler–Nordheim tunneling mechanism from gate injection. In this P/E voltage condition, a large memory window (~4.2 V) was observed by current–voltage measurement. Then, the speed and voltages of P/E were measured and discussed completely. The data retention of the Ni-NC assisted MANOS-LTPS-TFT-NVM is extracted to be 1.62 V of memory window after 10⁶ s.

1. Introduction

Recently, low-temperature polycrystalline silicon (poly-Si) thin-film transistors nonvolatile memory (LTPS-TFT-NVM) has been widely studied for applications in system-on-panel (SOP) and three-dimensional (3D) stacked memory devices.¹,² For these applications, TFT-NVMs will be required components in the future. However, a common problem of the LTPS-TFT-NVMs is their low programming/erasing (P/E) efficiency owing to the high operating voltage across the gate stack needed to program or erase carriers.³ To achieve a high P/E efficiency, metallic nanocrystals (NCs) embedded in NVMs have also been widely studied, which possess several advantages, such as a larger charge of capacity, a wider range of available work functions, a higher density of states around the Fermi level, and a smaller energy perturbation due to carrier confinement.⁵-¹³ Furthermore, as compared with semiconductor NCs, there is almost no voltage drops over metallic NCs owing to their good electrical conductive characteristics. Hence, low P/E voltage devices can be achieved by using metallic NCs as trapping centers. In this study, Ni-NCs embedded in metal–alumina–nitride–oxide–silicon (MANOS) TFTs were proposed for low P/E voltage NVM applications. Because Ni-NCs produce more trapping centers to capture electrons or holes, a large memory window can be obtained at low P/E voltages.¹⁴ Furthermore, the trapped carriers are injected from the metal gate through the Al₂O₃/Si₃N₄ asymmetric tunnel barrier (ATB),¹⁵,¹⁶ which also causes the high P/E efficiency at low operating voltages. Most importantly, the formation temperature of Ni-NCs is compatible with the LTPS-TFT process and suitable for realizing SOP applications in the future.

2. Experimental Methods

Figure 1 shows the MANOS-TFT-NVM device structure with the embedded Ni-NCs. The fabrication of the TFT-NVM was started by oxidizing a Si substrate in water vapor at 1000 °C to form a 500-nm-thick SiO₂ layer to simulate the isolation layer. A 100-nm-thick amorphous Si layer was then deposited on the SiO₂-coated wafer at 550 °C by low-pressure chemical vapor deposition. It was followed by annealing at 600 °C for 24 h in N₂ atmosphere to crystallize the amorphous Si to form a poly-Si/SiO₂/Si structure stack. The 500-nm-thick field isolation oxide layer was then deposited on the stack by plasma-enhanced chemical vapor deposition (PECVD), and the source and drain regions were then formed by patterning and etching the field isolation oxide layer. Then, the regions were implanted with phosphorus (35 keV, 5 × 10¹⁵ cm⁻²) and activated at 600 °C for 24 h in N₂ atmosphere. After patterning, the activation regions were followed by SiO₂/Si₃N₄ (5 nm/3 nm) gate stack deposition to form a Si₃N₄/SiO₂/poly-Si/SiO₂/Si stack by PECVD with SiH₄, NH₃, and N₂O as reaction gases. For NC formation, an approximately 4.5 nm wetting layer of pure nickel was deposited on the stack by electron-gun evaporation system deposition, which was followed by rapid thermal annealing (RTA) treatment to form the Ni-NCs at 550 °C. The distribution and morphology of Ni-NCs were manipulated by varying the process parameters. On top of NCS, a thin layer of Si₃N₄ (<2 nm) and a 5 nm Al₂O₃ were deposited by PECVD and the electron-gun evaporation system. The TFT-NVM devices were completed by gate definition with solution etching (H₃PO₄ : HNO₃ : CH₃COOH : H₂O = 50 : 2 : 10 : 9), con-

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Fig. 2. (Color online) SEM morphologies of the rapid thermal annealed Ni-NCs on Si$_3$N$_4$ layer for 1 min treatment time. The number density of Ni-NCs at 550 °C annealing for 1 min is about 5 × 10$^{11}$ cm$^{-2}$.

Fig. 3. Typical TEM cross-sectional image of Al$_2$O$_3$/Si$_3$N$_4$/Ni-NCs/Si$_3$N$_4$/SiO$_2$/poly-Si stack indicating the layer structures. There are some black dots in this figure that represent Ni-NCs.

Fig. 4. (Color online) $I_D$–$V_G$ curves of MANOS-TFT-NVMs with Ni-NCs at programming/erasing biases of −10 V for 1 s and +8 V for 1 s, respectively. The $V_{TH}$ shift of the device is about 4.2 V and the on/off current ratio can increase by up to 5 orders of magnitude with an on-current of 6 × 10$^{-6}$ A and the values of the subthreshold swing (SS) can decrease down to ~0.85 V/decade.

Fig. 5. (Color online) $I_D$–$V_G$ curves of MANOS-TFT-NVMs with Ni-NCs at programming/erasing biases of −10 V for 1 s and +8 V for 1 s, respectively. The $V_{TH}$ shift of the device is about 4.2 V and the on/off current ratio can increase by up to 5 orders of magnitude with an on-current of 6 × 10$^{-6}$ A and the values of the subthreshold swing (SS) can decrease down to ~0.85 V/decade.

3. Results and Discussion

After the 550 °C RTA treatment for 1 min, Ni-NCs were self-assembled on the Si$_3$N$_4$ layer from an ultrathin nickel film. The oxidizing possibility of Ni in the fabrication process should be decreased by using a vacuum RTA system with a N$_2$ atmosphere. A top-view SEM micrograph of Ni-NCs at programming/erasing biases of −650 V for 1 s and +10 V for 1 s, respectively. The oxidizing possibility of Ni in the fabrication process should be decreased by using a vacuum RTA system with a N$_2$ atmosphere.

Contact formation, Al electrode patterning, and 400 °C sintering. The gate length and width of the device are 10 and 100 μm, respectively. Finally, the Ni-NC-assisted MANOS-TFT-NVMs were characterized and analyzed by scanning electron microscopy (SEM), transmission electron microscopy (TEM), and current–voltage ($I$–$V$) measurements.

The large memory window should be caused by the hetero-interface of defect states between the NCs and the silicon-base dielectric layer. A schematic energy band diagram of the Al/Al$_2$O$_3$/Si$_3$N$_4$/Ni-NCs/Si$_3$N$_4$/SiO$_2$/poly-Si stack under equilibrium state is shown in Fig. 5(a). As compared with SiO$_2$, the narrow energy band-gap of Al$_2$O$_3$ causes the electron to easily pump into the energy well from the metal gate. Figure 5(b) shows the schematic band diagrams in the

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the issues causing electrons to tunnel from the metal gate more easily than from the poly-Si channel.

Figure 4 shows $I_D$–$V_G$ curves of the MANOS-TFT-NVM with Ni-NCs and with gate P/E biases of −10 and +8 V, respectively, for 1 s. The on/off current ratio can increase by up to 5 orders of magnitude with an on-current of 6 × 10$^{-6}$ A and the value of the subthreshold swing (SS) can decrease down to ~0.85 V/decade, signifying a rapid response of the device and a low leakage current of the poly-Si channel. The large memory window should be caused by the hetero-interface of defect states between the NCs and the silicon-base dielectric layer.
programming process. With a negative gate bias, electrons are injected to Ni-NCs by Fowler–Nordheim (FN) tunneling through the $\text{Al}_2\text{O}_3$/Si$_3$N$_4$ ATB structure. In reverse, with a positive gate bias, holes tunnel from the Al electrode through the tunneling layer and recombine with the electrons (not shown).

The $V_{TH}$ versus $V_G$ characteristics of the TFT-NVM are shown in Fig. 6(a). The data exhibits a uniform increment step pulse rate for both programming and erasing as the P/E voltages vary, which is a desirable feature for reliable P/E operation. This indicates that the MANOS-LTPS-TFT with Ni-NCs displays good P/E efficiency at low stress voltages. In Fig. 6(b), the device is tested by different stressing times with a constant voltage. Nevertheless, the trapping efficiency is disappointing at lower stressing times owing to the limitation of FN tunneling.

The two curves of retention time versus $V_{TH}$ for MANOS-TFT-NVMs with Ni-NCs in the device at room temperature are shown in Fig. 7 for two different states. These curves show that the $\sim1.62$ V memory window with a P/E condition of $-8/+10$ V, 1 s can be maintained for a retention time of $10^4$ s. The trade-off between good data retention and high P/E efficiency is the main issue of NVMs. In general, data retention can be extended by increasing the thickness of tunneling layers or improving the quality of tunneling layers. Furthermore, NCs embedded in the TFT-NVM device can also improve the storage of electrons through minimizing Frenkel–Poole leakage. This may be because the trapped electrons can be distributed and stored in many independent NCs. Each NC is insulated by a dielectric and the possibility of simultaneous leakage is minimized by this distributed storage structure. In addition,
Ni-NCs and Si$_3$N$_4$ layers also play important roles to prevent the trapped electrons tunneling out owing to the high work-function of nickel (≈5.15 eV) making a deep energy well$^{21}$ and the physical thickness of Si$_3$N$_4$ decrease the leakage current, respectively.

4. Conclusions

A Ni-NC-assisted MANOS-LTPS-TFT was fabricated and its performance demonstrated. It can be operated at low P/E voltage (−10/+/8 V) with a large memory window (~4.2 V). This result matches the future development of NVM, which needs a low power consumption and multi-bits cell application. The Ni-NCs assisted LTPS-TFT-NVM devices were fabricated on a SiO$_2$ substrate to simulate potential applications on glass panels and to extend the possibilities of applications in SOP and 3D stacked NVM.

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