Effects of RCA clean-up procedures on the formation of roughened poly-Si electrodes for high-density DRAMs' capacitors

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Received 20 December 1996; revised 19 May 1997; accepted 19 May 1997

Abstract

A novel structure, the phosphorus-implanted poly-Si films treated with phosphoric acid (H₃PO₄) and cleaned by standard RCA cleanup procedures, has been demonstrated as the bottom electrodes of DRAMs' stacked capacitors. After the H₃PO₄ treatment and RCA cleaning process, micro-island structures are formed on the poly-Si surface of the storage electrodes. The NH₄OH + H₂O₂ + H₂O (SC-1) solution in the RCA cleaning procedures is the main component to change the porous surfaces and engraved structures, formed by H₃PO₄ treatment, into micro-islands. Although the electrical properties are slightly degraded compared to the control samples, they fulfill the requirements of high-density DRAMs, resulting from the increment of cell capacitance.

Keywords: RCA clean-up procedures; Poly-Si electrodes; High-density DRAMs' capacitors

1. Introduction

To promote the density of dynamic-random-access-memories (DRAMs), the cell area in DRAMs' structures must be reduced. Reduction of cell capacitance, resulting from the memory cell miniaturization, is one of the most serious problems. Many advanced structures for the stacked capacitor cells have been investigated to enlarge the surface area of the storage electrodes so as to obtain sufficient cell capacitance [1-7]. Cylindrical storage electrodes, spread stacked electrodes, disk-shaped electrodes, micro villus patterning (MVP) electrodes, honeycomb-shaped electrodes engraved by the reactive-ion-etching (RIE) and uneven electrodes with hemispherical-grained (HSG) Si were demonstrated to meet this purpose of enlargement of effective surface area of the storage-node. However, it is difficult to carry out these complicated storage-node structures by use of conventional processes. Recently, Watanabe et al. [8] reported a new technique, in which in-situ phosphorus-doped poly-Si could be changed into a porous-Si through hot phosphoric acid (H₃PO₄) treatment. In this article, we observed that after H₃PO₄ etching and RCA cleaning processes, the phosphorus-implanted and activated poly-Si is changed into micro-island structures and the RCA clean-up procedures are the main cause to form these novel structures.

2. Experimental procedures

Capacitors with doped poly-Si bottom electrodes were fabricated on Si substrate covered with 3000 Å-thick SiO₂ which was grown at 1050°C in a steam ambient. Double poly-Si layers were used in this work to avoid the poly-Si lines broken when they were immersed into hot phosphoric acid (H₃PO₄). A 1000 Å-thick LPCVD poly-Si was deposited at 620°C and then phosphorus-implanted with 30 KeV, 4X10¹⁰ cm⁻² and annealed at 850°C for 30 min. After the native oxide was removed, some wafers were etched by 85% phosphoric acid (H₃PO₄) at 120°C for 150 min. Some of these wafers etched by H₃PO₄ were cleaned by standard RCA clean-up procedures and some were cleaned by H₂SO₄ + H₂O₂ (SPM), NH₄OH + H₂O₂ + H₂O (SC-1), HCl + H₂O₂ + H₂O (SC-2) respectively. The morphology of bottom electrodes were inspected by SEM. The capacitors being used to extracting electrical properties were formed by the following processes. Prior to the dielectric films formation, all of these wafers which were etched and unetched by H₃PO₄ were cleaned by standard RCA clean-up procedures. A 60 Å-thick nitride films were deposited at 750°C by LPCVD using the SiH₄/Cl₂/N₂ mixture and then all of these samples were oxidized at 850°C for 30 min in O₂.
ambient. A 2700 Å-thick poly-Si was deposited as the top electrodes and then POCl₃-doped at 850°C for 40 min and the sheet resistance which were measured by the four point probe was 40 ~ 50 Ωsq. Three-mask procedures were used to form the interpoly-Si capacitors and the cross-sectional structure was shown in Fig. 1. The electrical properties were measured by HP4150 and Keithly CV systems.

3. Results and discussion

Figs. 2 and 3 show the plain-view SEM micrographs of the phosphorus-implanted poly-Si electrodes without and with H₃PO₄ treatments, respectively. It was observed that after H₃PO₄ treatment, porous surfaces and engraved structures are formed on poly-Si grain surface and grain boundaries, respectively. But these structures cannot effectively increase the surface areas of the storage-nodes. The SEM micrograph of the samples etched by H₃PO₄ and cleaned by RCA clean-up procedures is shown in Fig. 4. It was found that micro-islands were formed on the poly-Si surface of the electrodes and there is a very big difference between Figs. 3 and 4. These micro-island structures can efficiently enlarge the surface areas of the storage electrodes. In order to distinguish which solutions in RCA clean-up procedures are the main causes, the H₃PO₄-etched samples are cleaned by H₂SO₄ + H₂O₂ (SPM), NH₄OH + H₂O₂ + H₂O (SC-1), and HCl + H₂O₂ + H₂O (SC-2) respectively, and the SEM images are shown in Figs. 5-7, accordingly. It can be seen that the images in Figs. 4 and 6 are almost the same shape, micro-islands on the surface of the electrodes. The coral-shaped poly-Si on the surface of the electrodes, which were only cleaned by H₂SO₄ + H₂O₂ or SC-2 respectively, are shown in Figs. 5 and 7. Because, in H₂SO₄ + H₂O₂ and SC-2 solutions, oxidation of poly-Si occurs on the surface owing to the component of H₂O₂ which has strong oxidizing capability. In SC-1 solution, not only oxidizing capability but also etching capability will attack to the H₃PO₄-etched surface of the poly-Si electrodes owing to the component of NH₄OH which will etch the silicon. The SC-1 is the dominant solution which change the porous-Si into micro-islands and increase the capacitance, resulting from the surface area enhancement of the storage-nodes. From C–V measurements, the capacitors with roughened and flat poly-Si possess the capacitance 18.17 fF μm⁻² and 5.77 fF μm⁻², respectively. The roughened poly-Si electrode can achieve the surface enlargement of 3.15 times. The electrical properties of the capacitors with these micro-islands as the bottom electrodes are shown in Figs. 8 and 9. The area of the testing capacitors is 3.14 x 10⁻⁴ cm². The leakage current density, which is defined as the leakage current divided by mask area, at +1.65 V and -1.65 V are 7.2 x 10⁻⁸ A cm⁻² and -3.3 x 10⁻⁸ A cm⁻², correspond-
The electrical properties are some degradation, as compared to the control samples, which result from the enlargement of surface area and the effect of field enhanced by the tips of micro-islands structures. However, they fulfill the requirements of future high-density DRAMS, owing to the large increase of cell capacitance. Weibull plots of TZDB characteristics under ramping voltage test also show some degradation, resulting from the enlargement of surface area and the effect of field enhanced by the tips of micro-islands structures. But owing to the much increment of cell capacitance, these capacitors could be used in future high-density DRAMS and those electrical properties could fulfill the requirements. The SC-1 is the dominant solution which changes the porous-Si into micro-islands. Therefore, this technique is promising for the future high-density DRAMS' applications.

4. Conclusions

In conclusion, the phosphorus-implanted poly-Si films etched by 85% phosphoric acid (H₃PO₄) and then cleaned with standard RCA clean-up procedures can simply and easily increase the surface areas of DRAMS' capacitors, i.e., increase the capacitance. The electrical properties, including leakage current density and TZDB characteristics, show some degradation, resulting from the enlargement of surface area and the effect of field enhanced by the tips of micro-islands structures. But owing to the much increment of cell capacitance, these capacitors could be used in future high-density DRAMS and those electrical properties could fulfill the requirements. The SC-1 is the dominant solution which changes the porous-Si into micro-islands. Therefore, this technique is promising for the future high-density DRAMS' applications.

Acknowledgements

This work was supported in part by the Republic Of China National Science Council (ROC, NSC) under Contract NSC-
The authors thank the National Nano Device Laboratory (NDL) of R.O.C. NSC and the Semiconductor Research Center (SRC) of National Chiao Tung University for technical support.

References


