1 fF ESD protection device for gigahertz high-frequency output ESD protection

J.-H. Lee, S.-C. Huang, Y.-H. Wu and K.-H. Chen

A mutual-protection scheme is proposed to achieve an ultra-low capacitance electrostatic discharge (ESD) protection device. The ESD protection device can not only dissipate ESD current, but also can make the vulnerable output transistor have the ESD protection capability. Namely, the output transistor can also protect ICs and help the ESD protection device to share the ESD current. Using this scheme can discharge more ESD current than the summation current of the two individual devices. From the ESD test result, it can achieve the required ESD level by using the ultra-low capacitance ESD protection device (\(~1.2 \text{ fF}\)).

Introduction: As technology advances to the nanometre regime, the ultra-thin gate oxide, ultra-short device channel length and ultra-shallow junction make the device more vulnerable to electrostatic discharge (ESD) stress than ever. Moreover, a transistor has the maximum loading capacitance limitation when it operates in the gigahertz (GHz) region for high frequency (HF) or radio-frequency (RF) applications [1]. To meet this criterion, the output transistor often does not have any ESD protection capability. The ESD performance of this kind of output transistor relies on the ESD protection device size. This makes it hard for the output transistor to reduce its loading capacitance if it needs to meet the required ESD level, 1 kV human-body model (HBM) and 30 V machine-model (MM) [2]. It has been reported that there are several schemes [3–7] that can improve the ESD performance of the fully silicided n-MOSFET to an excellent level. However, they all have their own limitations. Using the long contact-to-contact space [3] will increase the source/drain series resistance, which results in device RF characteristic degradation. The diode from I/O PAD to V_{DD} makes the substrate-trigger NMOS [4] and pnp-gate-driven NMOS [5] inapplicable for failsafe operation [6]. With a gate-booting capacitor, the n-MOSFET of the substrate-pump NMOS [6] cannot be used as the output transistor.

The diode string (DIOS) has been successfully used to lower the trigger voltage (V_{T1}) of the silicon-control-rectifier [7] below the breakdown voltage of the protected device. In this Letter, a DIOS is proposed to make the output transistor become the ESD protection device to share the ESD current with each other. So, this scheme is called the mutual-protection scheme.

Experiment: The technology used to fabricate the devices for this study is a 45 nm 1.1 V/2.5 V CMOS process and the architecture in this experiment is verified by using 1.1 V devices.

Structure: Fig. 1 shows the layout and cross-section of the structure used to implement the mutual-protection scheme. This structure is composed of an n-MOSFET, a DIOS and a p+ guard-ring. The n-MOSFET is the output transistor, which is a multi-finger device with 2 \(\mu\)m finger width, 100 \(\mu\)m total width and located at the centre of the p+ guard-ring. The DIOS is the ESD protection device, which is composed of three diodes in series and located at either side of the p+ guard-ring. The p+ diffusion area for each diode is 0.528 (0.33 \(\times\) 1.6) \(\mu\)m². From the spice model, the total capacitance of the DIOS is nearly 1.2 fF.

Fig. 2 shows the equivalent circuit of the structure in Fig. 1. For a p+/n-well diode fabricated on the p-substrate, it can be treated as a pnp bipolar transistor [8]. During the ESD zapping event, the pnp bipolar transistors of the DIOSs can provide the substrate currents to trigger the parasitic pnp bipolar transistors of the n-MOSFET. Thus, this structure is called the diode-triggered pnp (DTNPN).

High-current IV characteristics: Fig. 4 shows high-current IV characteristics of a total width 100 \(\mu\)m n-MOSFET, a DIOS and the DTNPN in Fig. 1. Below 1.7 V, the currents of the total width 100 \(\mu\)MOSFET and the DTNPN overlap each other and cannot be distinguished since the DIOS current is still too small to affect the current of the DTNPN. Above 2.1 V, the currents of the DTNPN and DIOS overlap each other and cannot be distinguished since the applied voltage is beyond the turn-on threshold voltage (V_T) of the DIOS. This implies that the DIOS does not lead to an increase in the current of the DTNPN output transistor under the normal 1.1 V operation. Moreover, the DIOS can also provide a current path to dissipate ESD current and trigger on the parasitic pnp bipolar transistor of the DTNPN output transistor during the ESD zapping event.

**Fig. 1** Layout for DTNPN

**Fig. 2** Equivalent circuit of DTNPN in Fig. 1

**Fig. 3** DC-IV characteristics of n-MOSFET, DIOS, and DTNPN in Fig. 1

**Fig. 4** High-current IV characteristics of n-MOSFET, DIOS, and DTNPN in Fig. 1
on before the snapback occurs. From Fig. 2, the DIOS is composed of the pnp bipolar transistors and the base current of one transistor injects into the emitter of the next stage pnp bipolar transistor as the emitter current. Moreover, all collector currents of the DIOS flow into the p-substrate and through the substrate resistors to raise the substrate potential. As the substrate potential is increased beyond 0.9 V [9], the diode D1 between the source terminal of the n-MOSFET and p-substrate terminal is biased at the high-injection region. This induces the source terminal to inject a lot of electrons into the high-field drain terminal to give rise to the substrate current generation due to the impact ionisations. Subsequently, the generated substrate currents combined with the collector currents of the DIOS can sustain enough substrate potential to bias the source terminal at the high-injection region. Thus, the source can keep injecting the electrons to the drain terminal to generate the substrate current. These actions form a loop to cause the nnp bipolar of the DTNPN n-MOSFET to turn on and drive it into the snapback region. The snapback voltage \( V_{t1} \) and \( V_{t2} \) of the DTNPN are smaller than the \( V_{t1} \) or a pure n-MOSFET, about 2.1 and 1.2 V, respectively. This prevents the high voltage from damaging the DTNPN n-MOSFET during the ESD zapping event. Unlike the pure n-MOSFET, the DTNPN n-MOSFET is not damaged after the first snapback and its \( I_{t2} \) (\( \approx 0.16 A \)) is apparently much higher than the DIOS \( I_{t2} \) (\( \approx 0.16 A \)). This implies that the DIOS can make the DTNPN n-MOSFET have the ESD protection capability to resist the ESD damage. Furthermore, the DTNPN n-MOSFET can also protect the DIOS from ESD damage since the voltage drops down by about 0.9 V beyond its \( V_{t1} \). Because of the npn bipolar turning-on, the voltage will be clamped at the low snapback voltage and will not damage the DTNPN until it rises beyond the \( V_{t1} \) of the pure n-MOSFET. This phenomenon, that the DIOS and n-MOSFET protect each other alternately, is called the mutual-protection scheme. Using this scheme, the ESD protection device can be minimised since ESD will not damage the DIOS even though its \( I_{t2} \) is only slightly higher than the \( I_{t1} \) of the DTNPN. After turning on, the n-MOSFET can dissipate most ESD current. From the ESD test result, the DTNPN can pass 1.0 KV HBM and 50 V MM even though the total capacitance of its ESD protection device is only 1.2 ff.

**Conclusion:** Using the conventional ESD protection scheme, it is very difficult to reduce the capacitance of the ESD protection device to the femtofarad range if it still needs to meet the required ESD level. The mutual-protection scheme provides an easy way to achieve the capacitance of the ESD protection device for the output transistor into the femtofarad range.

© The Institution of Engineering and Technology 2011
20 June 2011
One or more of the Figures in this Letter are available in colour online.
S.-C. Huang and K.-H. Chen (Institute of Electrical and Control Engineering, National Chiao Tung University, Taiwan)
E-mail: ajakes2010.cee95g@nctu.edu.tw
J.-H. Lee (ESD/Latch-up independent consultant for Richtek Technology Corporation and Realtek Semiconductor Corporation)
Y.-H. Wu (Realtek Technology Corporation)

**References**
1 Richier, C., Salome, P., Mab gouxs, G., Zaza, J., Juge, A., and Mortini, P.: ‘Investigation on different ESD protection strategies devoted to 3.3V RF application (2GHz) in a 0.18 μm CMOS process’. Proc. 22nd EOS/ESD Symp., Anaheim, CA, USA, 2000, pp. 251–259
2 Industry Council on ESD target level, ‘White paper 1: A case for lowering component level HBM/MM specifications and requirements’, October 2010

ELECTRONICS LETTERS 1st September 2011 Vol. 47 No. 18