A New Approach to Modeling the Substrate Current of Pre-Stressed and Post-Stressed MOSFET's

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Abstract—In this paper, we propose a closed form expression of a new and accurate analytical substrate current model for both pre-stressed and post-stressed MOSFET's. It was derived based on the concept of effective electric field, which gives a more reasonable impact ionization rate in the lucky-electron model. This effective electric field, composed by two experimentally determined parameters, can be regarded as a result of nonlocal heating effects within devices. This model shows a significant improvement to the conventional local field model. One salient feature of the present model is that it allows us to characterize the time evolution of the substrate current of stressed MOSFET's for the first time. Experimental verification for a wide variety of MOSFET's with effective channel length down to 0.3 µm shows that the new model is very accurate and is feasible for any kind of MOS device with different drain structures. The present model can be applied to explore the hot carrier effect in designing submicrometer MOS devices with emphasis on the design optimization of a device drain engineering issue. In addition, the present model is well suited for device reliability analysis and circuit level simulations.

I. INTRODUCTION

I

T is well known that the substrate current $I_B$ can be used as a good monitor of the hot carrier effect [1]. Therefore, accurate prediction of the substrate current is crucial in designing reliable MOS devices and for analyzing circuit level reliability in VLSI/UlSI design [2], [3]. In modeling the substrate current, the widely used form [4]-[6] for device analysis and circuit simulation utilizes the maximum electric field ($E_m$) in the local electric field for the specific device structure as the dominant factor in hot carrier generation. This local field model for the substrate current agrees reasonably well for large devices (e.g., $L_{eff} > 1.0 \mu m$). However, for the short channel MOS devices, the local field model fails to model the $I_B$ especially at high gate biases. To improve modeling accuracy, the impact ionization rate has to be modeled nonlocally by considering the two-dimensional (2-D) electric field effects as well as the heating effects [7], [8] (i.e., the solution by considering the nonthermal effect).

In addition to the drain current degradation in stressed devices, hot carrier induced oxide damages will in turn affect the inner channel electric field distribution which then alter the substrate current characteristics [9]. Due to the difficulty in knowing the exact information about the amount and distribution of interface states or oxide charges, none has been made to model the substrate current characteristics of stressed MOSFET's in analytical form. Undoubtedly, an accurate $I_B$ model for degraded devices is also essential for device and circuit level reliability studies.

To deal with the aforementioned problems, in this paper, we will propose a new analytical substrate current model based on the so-called effective electric field instead of the $E_m$ concept to calculate the impact ionization rate as well as the substrate current. Section II describes the new substrate current model and the new approach for modeling both the pre-stressed and post-stressed $I_B$ characteristics. Discussion and the comparison with reported models are also given. Section III presents a major application of this new model to study the hot carrier reliability of a new class of LATID (Large-Angle- Tilt Implanted Drain) MOS devices. Conclusions are given in Section IV.

II. A NEW ANALYTICAL SUBSTRATE CURRENT MODEL

In this section, a self-consistent analytical substrate current model for pre-stressed (fresh) and post-stressed MOSFET's was derived by combining the concept of Lucky-Electron (LE) model and nonlocal field effect within devices. A series of LDD and LATID MOS [10] devices with a wide range of process and device parameters, such as gate oxide thickness ($T_{ox}$), spacer width ($X_sp$), n+ implantation dosage and implantation angle, are used to justify the accuracy of the present model. All the devices in this study have drawn channel width ($W$) 20 µm.

A. A New Substrate Current Model for MOSFET

Based on the concept of the effective electric field, an improved $I_B$ model can be expressed as

$$I_B = \frac{\alpha}{\beta} I_D \cdot L_d \cdot E_{eff} \cdot \exp(-\beta/E_{eff})$$

$$= \frac{\alpha}{\beta} I_D \cdot (V_{DS} - V_{Dsat}) \cdot \exp(-\beta/E_{eff})$$

Here, the impact ionization rate $\alpha = \alpha \cdot \exp(-\beta/E_{eff})$ is used, in which $E_{eff}$ is used instead of $E_m$ in the conventional LE model. In the LE model, $E_m$ is expressed as $(V_{DS} - V_{Dsat})/L_d$ [4], where $V_{Dsat}$ is the saturation voltage. We define $E_{eff} = (V_{DS} - V_{Dsat})/L_d$ as the effective electric field inside a device.
that is decisive for hot carrier behaviors. \( I_d \) is regarded as the effective hot carrier distribution length. \((V_{DS} - V_{D\text{hot}})\) is considered as the hot carrier driving force, in which \( V_{D\text{hot}} \) is the hot carrier starting force. In developing this model, two-dimensional nonlocal field effect or the electron heating effect is included in the \( E_{\text{eff}} \) term which can be experimentally determined. To extract \( E_{\text{eff}} \), (1b) is rearranged to obtain another \( E_{\text{eff}} \) expression which gives

\[
E_{\text{eff}} = \frac{V_{DS} - V_{D\text{hot}}}{I_d} \quad (2a)
\]

\[
= \frac{1}{\beta} \ln \left( \frac{I_d - \alpha (V_{DS} - V_{D\text{hot}})}{I_0 \beta} \right) \quad (2b)
\]

For a given gate bias \( V_{GS} \) and from the measured \( I_{DS}-V_{DS} \) and \( I_B-V_{DS} \) curves, two important parameters, \( V_{D\text{hot}} \) and \( I_d \), can be uniquely obtained by taking the following steps:

1) To calculate saturation voltages \( V_{D\text{sat}} \) from \( I_{DS}-V_{DS} \) data, the method described in [11] was adopted here. In this method for determining \( V_{D\text{sat}} \), a function \( G \) is defined as

\[
G = g_{ds} \cdot \frac{\partial}{\partial V_{DS}} \left( \frac{1}{g_{ds}} \right) \quad (3)
\]

where \( g_{ds} = \partial I_{DS}/\partial V_{DS} \) is the conductance of the device. The first peak values of the \( G \) versus \( V_{DS} \) curves correspond to the saturation point where \( V_{DS} = V_{D\text{sat}} \). The \( V_{D\text{sat}} \) value will be used as the initial guess for undetermined parameter \( V_{D\text{hot}} \).

2) The surface impact ionization coefficients, \( \alpha \) and \( \beta \), adopt the values by Slotboom et al. [12] and are treated as fixed values in this model. With \( V_{D\text{hot}} \) initially guessed as \( V_{D\text{sat}} \), doing iteration between (2a) and (2b) using fixed point algorithm, \( V_{D\text{hot}} \) and \( I_d \) can be found. As (2a) implies, the relationship between \( E_{\text{eff}} \) versus \( V_{DS} \) exhibits a straight line. The intercept of the line with the \( V_{DS} \) axis and the slope give \( V_{D\text{hot}} \) and \( I_d \) values.

For different gate voltages, Fig. 1 shows the linear relationship between \( E_{\text{eff}} \) and \( V_{DS} \) for an LDD device, in which \( I_{on} \) and \( I_{off} \) represent the drawn channel length and effective channel length, respectively. \( V_{D\text{hot}} \) and \( I_d \) are found to be increasing functions of \( V_{GS} \) and can be expressed as an empirical form easily. The comparison of the \( I_g \) characteristics given in Fig. 2 between the modeled and measured results for different channel length devices shows excellent agreements for wide range biases. Fig. 3 shows excellent agreements between modeled and experimentally measured \( I_B \) characteristics for both LDD and LATID MOS devices with wide range of gate oxide thickness, \( n^- \) implantation dosage and angles. In particular, the effective channel length of the device in Fig. 3 (marked with solid triangle) with \( n^- \) dosage 6E13 cm\(^{-2}\) and 45° implantation angle is 0.3 \( \mu \)m (extracted using the method described in [13]). One distinct feature of this new approach is that \( V_{D\text{hot}} \) and \( I_d \) are self-consistently extracted from experimental data so that very accurate modeled results can be achieved. Moreover, no additional fitting procedure is needed.
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stress on devices. The device was first biased at $V_{GS} = 1$ V and $V_{DS} = 7$ V for $10^5$ seconds stress, then, subsequently biased at $V_{GS} = 7$ V for another $10^5$ seconds stress. The device characteristics were measured during certain period of the stress time. A fixed base level charge pumping measurement [14] was also performed to identify the types of the oxide damages after carrier injection.

1) $E_{eff}$ Variation During Hot Hole Injection: Devices stressed at $V_{GS} = 1$ V and $V_{DS} = 7$ V will cause hole injection, since the direction of the momentum of holes is toward the gate while electron is to the drain. The hole injection generates hole traps in the oxide as identified by charge pumping method, similar measurement results were also observed and well explained in [9]. The time evolution of parameters $V_{DHot}$ and $I_d$ for a LDD device during hot hole injection are shown in Fig. 4. $V_{DHot}$ values vary slightly, while the $I_d$ values increase with stress time and the $I_d-V_{GS}$ curve shift in parallel, the resultant $E_{eff}$ decreases. In other words, hole traps reduce the $I_d$ current. Using the extracted parameter values, the modeled $I_d$ characteristics of a post-stressed device and the comparison with experiment for two successive stress time are given in Fig. 5 which shows excellent agreement. The new model successfully characterizes the $E_{eff}$ variations.

2) $E_{eff}$ Variation During Hot Electron Injection: The same device was continuously biased at $V_{GS} = V_{DS} = 7$ V for additional stress to generate hot electron injection. Judging from charge pumping measurement, the latter electron injection generates large amount of positive charges, which can be negative oxide traps and acceptor-type interface states as explained in [9]. The time evolution of $V_{DHot}$ and $I_d$ during hot electron injection was evaluated and a similar result to Fig. 4 was obtained. The $I_d-V_{GS}$ curve shifts parallelly, however, the $I_d$ values decrease with stress time in contrast to the effect of aforementioned hole injection. The $V_{DHot}-V_{GS}$ curve merely increasingly shifts to a relatively large value (0.03 V in this case) in a very short time (less than 50 seconds) stress and then almost unchanged in the following stress, the resultant $E_{eff}$ increases with stress time. In other words, negative oxide traps and acceptor-type interface states enlarge $I_d$.

3) The $E_{eff}$ Variation of Post-Stressed MOSFET's in Reverse Mode Operation: The reverse mode $I_d$ characteristics (exchanging source and drain electrodes) were also characterized to study the influence of source side oxide damages on the
hot carrier behaviors. The stress was done at \(V_{GS} = 1\) V and \(V_{DS} = 7\) V for \(10^4\) seconds. The parameters \(V_{Dhot}\) and \(\lambda_d\) show very different variations with stress time and \(V_{GS}\) as compared with the aforementioned two forward mode cases. \(V_{Dhot}\) values increase especially at higher \(V_{GS}\) biases. On the contrary, \(\lambda_d\) values decrease gradually with increasing \(V_{GS}\). Higher gate bias magnifies the oxide damage effect at the source side. Longer stress time has larger variations. The resultant effect of the source side oxide damages reduce \(E_{eff}\), and thereby giving rise to the decrease of \(I_B\) with stress time. The reverse mode \(E_{eff}\) of LDD devices has larger degradation than that of LATID devices which will be explained later.

C. Discussion

Several implications from the comparison of the present model with the conventional ones [4]-[6] can be drawn as follows:

1) In modeling the substrate current of a conventional single drain MOS device, the following form of the conventional approach [5] based on the local field concept is widely used

\[
I_B = \frac{\alpha}{\beta} I_D \cdot \lambda_d \cdot E_m \cdot \exp(-\beta/E_m) \quad (4a)
\]

\[
= \frac{\alpha}{\beta} I_D \cdot (V_{DS} - V_{Dsat}) \cdot \exp(-\beta \lambda_d/(V_{DS} - V_{Dsat})), \quad (4b)
\]

in which \(E_m = (V_{DS} - V_{Dsat})/\lambda_d\) is generally considered as the maximum electric field along the channel. Two approaches are commonly used to calculate \(E_m\). (a) \(V_{Dsat}\) is extracted experimentally by utilizing the idea implied in (4b) as first described in [5], and the \(\lambda_d\) is presumably formulated related to the device geometry [15] which is treated as the characteristic length that is bias independent. In this approach to model \(I_B\), \(\alpha\) and \(\beta\) values can be extracted experimentally from (4b) as long as \(V_{Dsat}\) and \(\lambda_d\) have been calculated. (b) The \(E_m\) value and its expressions are obtained or fitted from device simulation or analytical electric field models [4], [6]. The modeled results of (4b) using approach (a) are compared with the new model and the measured data as shown in Fig. 2. Since the model parameters are not all directly extracted from experimental data self-consistently, the above approaches more or less require adjustable parameters (e.g., \(\alpha\) and \(\beta\)) to reasonably match their models with measured data. However, their results often mismatch the \(I_B\) values at higher \(V_{GS}\) values since their \(E_m\) expressions fail to reflect the complicated electric field variations over wide biases. In the new approach here, \(E_{eff}\) really reflects the 2-D electric field effect so that the overall impact ionization rate \(\alpha \cdot \exp(-\beta/E_{eff})\) accurately determines the \(I_B\) value.

2) One salient feature of the new approach is that it can be applied to any kind of MOS devices with different drain structures (e.g., LDD, LATID devices). However, the conventional approaches to obtained \(E_m\) were derived based on the conventional single drain MOS devices only, and needs individual modification for different LDD structures.

3) The extracted \(V_{Dhot}\) is smaller than its initial guess \(V_{Dsat}\). For the first time, this model suggests that the hot carrier driving force should be \((V_{DS} - V_{Dhot})\) instead of widely used value \((V_{DS} - V_{Dsat})\) which reflects only maximum electric field. In other words, the \(E_m\) concept is not adequate to present 2-D effect inside devices.

4) Various stress experiments performed at different biases and devices show that the hot carrier induced oxide damages have minor effect on the overall apparent hot carrier driving force \((V_{DS} - V_{Dhot})\). However, \(\lambda_d\) is sensitive to the net amount of total trapped oxide charges. The parallel shift of \(\lambda_d\) curves in Fig. 4 can be characterized and empirically formulated as a function of time given by

\[
\Delta \lambda_d = 3.0712 \times 10^{-7} \cdot \log(t) \text{ (cm)}. \quad (5)
\]

With \(V_{Dhot}\) approximately unchanged, the stressed \(I_B\) characteristics (Fig. 5) can be predicted by employing (5) with very high accuracy.

5) During the hot carrier injection, large amount of interface states are generated below the sidewall spacer at the drain side which then in reverse mode operation electrically deplete mobile carriers at the source side and thus induce additional series resistance there. The variations of \((V_{DS} - V_{Dhot})\) and \(\lambda_d\) in reverse mode are caused by an extra voltage drop at the source side due to the increased series resistance which effectively decreases drain bias and gate bias. This resistance effect is more obvious at high \(V_{GS}\) biases, since the larger drain current enhances more larger voltage drop across the damaged region. Assume \(\Delta V(V_{GS})\) is the voltage dropped at source region, the effective gate bias excluding resistance effect reduces to \((V_{GS} - \Delta V(V_{GS}))\), which reduces the drain current. Owing to less amount of conducting carriers in the channel, the carriers in the
Comparison of $V_{D_{\text{Dest}}}$ and $V_{D_{\text{hot}}}$ on the $I_{DS}$-$V_{DS}$ curves for the same device in Fig. 1.

V. CONCLUSION

In this paper, a new concept for modeling the hot carrier induced MOS device substrate current is proposed. Three major improvements over the previous models are 1) an effective electric field is introduced in the model to account for the hot carrier heating and 2-D field (nonlocal) effects within devices; 2) the new analytical substrate current model is rather flexible and suitable for any kind of MOS devices with different drain structures; and 3) it enables us to model the post-stressed $I_B$ characteristics for the first time. This study also finds that different types of oxide damages show very different influences on the effective electric field. The post-stressed $I_B$ characteristics are skillfully modeled through characterizing the time evolution of effective electric field. The new approach accurately calculates the $I_B$ characteristics for MOS devices with effective channel length down to 0.3 μm.

One major application of the present model is to explore the hot carrier effect in designing a submicron MOS device with emphasis on the drain engineering issue. With a trade-off between the use of n+ implantation dosage and angle, we conclude that the design optimization of a hot carrier...
resistant LATID device can be better understood through the use of the newly developed substrate current model. The newly developed substrate current model can be further incorporated into SPICE models to evaluate the circuit level hot carrier reliability [18].

REFERENCES


Steve Shao-Shiun Chung (S'83-M'85) received the B.S. degree from the National Cheng-Kung University, Taiwan, in 1973, the M.Sc. degree from the National Taiwan University in 1975, and the Ph.D. degree from the University of Illinois at Urbana-Champaign, in 1985, all in electrical engineering.

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