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Effect of Gate Length on Device Performances of AlSb/InAs High Electron Mobility Transistors Fabricated Using BCl₃ Dry Etching

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Electronic and optical devices based on binary alloys of the 6.1 Å family including InAs (6.058 Å), GaSb (6.096 Å), and AlSb (6.136 Å) have attracted much attention recently. Antimonide-based compound semiconductor AlSb/InAs high electron mobility transistors (Sb HEMTs) have been demonstrated for extremely low voltage operations due to the combination of high peak electron velocity (~4 × 10⁷ cm/s) at a low electric field and high channel conductivity with the high electron confinement barrier (1.35 eV) of the InAs/AlSb interface. In this study, we fabricate AlSb/InAs and InAlAs stacked layers to prevent air exposure and provide a metamorphic buffer layer. BCl₃ gas has been found to be more effective for etching AlGaSb applying chlorine-based gases. The critical step in guaranteeing the success of AlSbInAs HEMTs is mesa formation through a novel inductively coupled plasma (ICP) process using BCl₃ gas (ULVAC NE-950EX etcher) and the dry etching was stopped at the AlSb barrier layer to attain high electron transfer efficiency and reduce the gate-to-channel distance. A 5-nm-thick In₉Ga₃Al₉Sb₃Sb layer was capped on the GaSb and AlSb layers to prevent air exposure and provide a chemically stable surface layer. The electron sheet carrier density and mobility at room temperature were measured to be 1.7 × 10¹⁵ cm⁻² and 22,400 cm² V⁻¹ s⁻¹, respectively.

In this paper, we present the development of a mesa isolation process for AlSb/InAs high electron mobility transistors (HEMTs) using inductively coupled plasma (ICP) etching with BCl₃ gas. Devices with different gate lengths (Lg = 60, 100, and 200 nm) fabricated by this dry etching technique show good DC and RF performances. With an appropriate Lg/gate-channel distance ratio, the 200-nm-gate has very high peak transconductances of 781 mS/mm at VDS = 0.1 V and 2000 mS/mm at VDS = 0.5 V. Moreover, an extrinsic current gain cutoff frequency of 137 GHz and maximum oscillation frequency of 97 GHz were achieved at a drain bias voltage VDS = 0.3 V, indicating the great potential for such a device operating at high frequency with extremely low DC power consumption. © 2012 The Japan Society of Applied Physics

Fig. 1. Epitaxial structure of the AlSb/InAs HEMT device. The inserted SEM image is the T-shaped gate after silicon nitride passivation. Devices with Lg between 60 and 200 nm were fabricated.
gas. The etching rate is well controlled to obtain shallow mesa isolation. The measured etch depth as a function of the etching time with Cl$_2$/Ar mixed gas is depicted in Fig. 2(b). As observed from the figure, it is hard to control the etching depth using Cl$_2$/Ar due to the drastic increase in depth when the etching time is approximately 200 s. The depth of the device mesa was measured to be approximately 1500 Å by KLA-Tencor P-10 surface profiler. Pd/Pt/Au ohmic contacts were evaporated and subsequently annealed at 300 °C for 30 s in N$_2$ ambient, resulting in a low contact resistance of 0.027 Ω-mm and a sheet resistance of 157 Ω/sq.

Non-recessed Pt/Ti/Pt/Au T-shaped gates were defined on the InAs cap layer using trilayer resist and electron beam lithography. The inserted scanning electron microscopy (SEM) image in Fig. 1 is the 60 nm T-shaped gate after silicon nitride passivation. Finally, a 100-nm-thick SiN passivation layer was deposited by low-temperature plasma-enhanced chemical vapor deposition (PECVD) to protect the devices.

Figure 3(a) shows the drain–source current ($I_{DS}$) as a function of drain–source voltage ($V_{DS}$) with the gate–source voltage ($V_{GS}$) varied from 0 to −0.8 V for the 200-nm-gate and 2 × 20-μm$^2$-width device. The device exhibits a maximum drain current density of 900 mA/mm at a gate bias of 0 V and a drain bias of 500 mV. Figure 3(b) shows the DC transconductance ($g_{m}$) as a function of gate voltage at different $V_{DS}$ for the same device. A maximum DC $g_{m}$ of 2000 mS/mm is achieved at the same bias. At room temperature, the measured on-resistance $R_{ON}$ was 0.33 Ω-mm.

The IV characteristics in Fig. 3 illustrate the advantages of the Sb HEMT with low-voltage operation, low $R_{ON}$, and high $g_{m}$, which are necessary for ultralow-power and high-frequency applications. Such a high current density and $g_{m}$ value result from the high peak electron velocity at a low electric field and the high channel conductivity, which enable the operation of AlSb/InAs HEMTs at very low drain bias voltages. As observed from Fig. 3(b), the drastic increase in the $g_{m}$ peak value for $V_{GS}$ greater than 0.4 V is due to the impact ionization in the channel resulting from the staggered band lineup at InAs/AlSb heterojunctions. Since the staggered band alignment at such heterojunctions does
not confine holes, electron flows into the channel, increasing the channel current and $g_m$.\(^\text{(10)}\)

The transconductance and drain–source current plotted as a function of gate voltage for devices with different gate lengths at $V_{DS} = 0.3\, \text{V}$ is shown in Fig. 3(c). The peak $g_m$ of the 200 nm device (1401 mS/mm) is slightly higher than those of the 100 nm (1288 mS/mm) and 60 nm (1329 mS/mm) devices.

The $S$-parameter of the devices was measured from 2 to 110 GHz using an on-wafer probe system with an HP8510XF network analyzer. The extrinsic cutoff frequency ($f_T$) and maximum frequency of oscillation ($f_{\text{max}}$) were extracted from extrapolation of the measured current gain ($H_{21}$) and Mason’s unilateral gain ($U$) using a $-20\, \text{dB/decade}$ slope. The 200 nm device exhibited $f_T$ and $f_{\text{max}}$ of 137 and 97 GHz at $V_{DS} = 0.3\, \text{V}$, respectively. These results also demonstrate the feasibility of BCl\(_2\) dry etching for shallow mesa formation in Sb HEMTs fabrication.

$f_T$ as a function of gate voltage for different gate lengths is shown in Fig. 4. As shown, high $f_T$ and $f_{\text{max}}$ were achieved at low bias levels for all devices due to the good transport properties in the InAs channel. Interestingly, it is observed that the 60 nm device does not significantly outperform the others as expected. The extracted intrinsic RF $g_m$ was 1250 mS/mm for the 60 nm device, 1175 mS/mm for the 100 nm device, and 1225 mS/mm for 200 nm device, which showed a similar trend to that depicted in Fig. 4. Apparently, merely scaling the gate length is not enough to boost the $f_T$ if the gate-channel distance is not optimized with the $L_g$ aspect ratio, which agrees with the results of Guerra et al.\(^\text{(11)}\) Another reason for this phenomenon is the occurrence of the ballistic effect in the electron transport under the gate electrode for the 60 and 100 nm devices.\(^\text{(12)}\)

In summary, an ICP dry etching process using BCl\(_2\) gas has been developed to precisely control the etching depth for shallow mesa isolation in the fabrication of AISb/InAs HEMTs. Effect of the gate lengths on device performances was also investigated. Good DC and RF performances, with an extrinsic $f_T/f_{\text{max}}$ of 137/97 GHz, were achieved at $V_{DS} = 0.3\, \text{V}$ for $2 \times 20\, \mu\text{m}$ HEMTs with a 200 nm gate length. These results demonstrate the potential of Sb HEMTs for low-voltage operation at high frequencies.

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