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This letter studies the channel hot carrier stress (CHCS) behaviors on high dielectric constant insulator and metal gate HfO$_2$/TiN p-channel metal-oxide-semiconductor field effect transistors. It can be observed that the degradation is associated with electron trapping, resulting in Gm decrease and positive Vth shift. However, Vth under saturation region shows an insignificant degradation during stress. To compare that, the CHC-induced electron trapping induced DIBL is proposed to demonstrate the different behavior of Vth between linear and saturation region. The devices with different channel length are used to evidence the trapping-induced DIBL behavior.

The physical limitation of the silicon dioxide (SiO$_2$) as gate insulator has achieved the point where its thickness is approaching to a few atomic layers thick. Below the physical thickness 12 Å, the significant gate leakage current results in a volume active power consumption, leading a worse reliability of metal-oxide semiconductor field effect transistors (MOSFETs). To avoid this serious issue, high-k dielectrics have been introduced as hafnium (Hf)-base, zirconium, aluminum oxides and heavily investigated as a replacement for conventional SiO$_2$ gate insulator. However, high-k/metal gate stack has to face many critical issues such as defects in high-k material which can lead to undesired transport through the dielectrics and trapping-induced instabilities.

As MOSFETs scaling down, not only the BTI reliability at gate terminal but also hot carrier effect (HCE) which is associated with lateral electric field is important issue in MOSFETs. Therefore, hot carrier effect in high-k/metal gate n-MOSFETs was still one of major device reliability concern. As is well known, under hot carrier injection, a high lateral electric field in pinch-off region accelerates the electrons sufficiently to gain enough energy to damage the drain side, resulting in the degradation of I-V characteristics. However, most of the studies were concentrated on n-MOSFETs. The degradation due to hot carrier effect in p-MOSFETs with high-k/metal gate stacks has not received as much attention. Therefore, the aim of this letter is to investigate the effects of channel hot carrier stress (CHCS) on HfO$_2$/TiN p-MOSFETs. It was found that the CHC-induced electron trapping dominates the degradation during stress, instead of interface states (Nit) creation, including Vth shift and Gm decrease. As the drain voltage (Vd) was applied at saturation region, there is no significant Vth shift during stress. This behavior was doubted to result from trapping-induced drain-induced-barrier-lowering (DIBL). To explain this phenomenon, the device with different channel length (L) was introduced to support our model in this work.

The HfO$_2$/TiN p-MOSFETs were studied in this paper based on the high-performance 28-nm CMOS technology. Both devices were fabricated using a conventional self-aligned transistor flow through the gate first process. For the gate first process devices, 10 Å and 30 Å of high quality thermal oxide were, respectively, grown on a (100) Si substrate as buffer oxide layers. After standard cleaning procedures, 30 Å of HfO$_2$ films were sequentially deposited by atomic layer deposition. Next, 10 nm of TiN films were deposited by radio frequency physical vapor deposition, followed by poly-Si deposition as a low resistance gate electrode. The source/drain and poly-Si gate activation were performed at 1025 °C. In this study, the dimensions of the selected devices were 10 μm and 1 μm in width and length, respectively. The device with buffer thickness of 10 Å was subjected to the maximum substrate current of CHCS conditions with −3.6 V drain voltage (Vd). The stress was briefly interrupted to measure the drain current-voltage (I$_d$-V$_d$) and substrate current-voltage characteristics. The gate induced drain leakage (GIDL) current was defined under the Vg = 0.5 V and Vd = −2.4 V. All experimental curves were measured using an Agilent B1500 semiconductor parameter analyzer.

The drain current-gate voltage (I$_d$-V$_g$) and substrate current-gate voltage (I$_b$-V$_g$) transfer characteristics. The gate induced drain leakage (GIDL) current was defined under the Vg = 0.5 V and Vd = −2.4 V. All experimental curves were measured using an Agilent B1500 semiconductor parameter analyzer.
(Vth), respectively. And ID seems to be invariant at V_G = -1.6 V. Generally, the behavior of CHC effect on n-MOSFETs has a cruel degradation at drain side due to impact ionization, decreasing in ID and Gm, but Vth shift is insignificant unless Nit generation due to higher lateral electric field during CHCS, respectively. However, the Vth shift toward positive direction is obtained under CHCS for high-k/Metal gate p-MOSFETs as shown in Fig. 1. We suggest that Vth shift and decrease in Gm could result from electron trapping in high-k layer during stress. When electron-hole pairs are produced by impact ionization, the stressing potential difference between gate and drain (VGD) makes electron tend to inject to gate side, resulting in Vth shift. Simultaneously, the field-effect mobility (Gm) is also influenced by charge trapping, enhancing the channel scattering. However, Vth shift due to electron trapping should make ID increasing, but the scattering reduces the channel-mobility and decreases ID. Because those two causes are antagonistic in ID then resulting an invariant in ID. Additionally, the inset of Fig. 1 shows the ID-VG curve under semi-logarithmic scale before and after CHCS. It can be found that the degradation of subthreshold slope (SS) is insignificant, illustrating the Nit is less. Therefore, this result supports our assumption that the degradation of Vth is induced by electron trapping in high-k layer located at drain side, instead of CHC-induced Nit. In order to solid the claim, the capacitance of gate terminal to drain terminal versus gate voltage (CGD-VG) curve shows the occurrence of electron trapping near drain side as shown in Figure 2(b). It can be seen that the capacitance of gate terminal to source terminal versus gate voltage (CGS-VG) curve has no significant change before and after stress, demonstrating the degradation is located at drain side. As well as, those experimental data are consistent with the suggestion of degradation which is dominated by CHC-induced electron trapping within drain side we declared. However, the occurrence of electron trapping at drain side still has insufficient justification to vary Vth with insignificant Nit generation. In order to comprehend how comes the Vth shift under CHCS, we extract the degraded tendency of Vth versus stress time in linear and saturation region, which are defined Lin-Vth and Sat-Vth, respectively. Figure 3 shows the CHCS degradation of Lin-Vth and Sat-Vth versus stress time. The Lin-Vth was extracted from Gmmax and corresponding gate voltage at ID = 10^-6 A as selected for Sat-Vth. It can be observed that an obvious shift on Lin-Vth, but Sat-Vth seem almost to be invariant under CHCS. As the result, the mechanism is deduced by trapping-induced DIBL. As electron-hole pairs are created by CHC impact ionization, CHC-induced electrons could be trapped into HfO2 layer within drain side, which has been evidenced previously. As electron trapping occurs, it could bend channel potential upward to help the linear VD (Lin-VD) to
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considered by choosing similar IBmax to control the same probability of trapping, the close impact ionization rate is amount of electron-hole pairs. Due to the 10 mA IBmax, the Lin-Vth shift under CHCS for HfO2/TiN p-MOSFETs with different channel length L. It can be found that the Lin-Vth shift has a positive shift on all the devices, regardless of different channel length. However, the Lin-Vth shift has a negative related to channel length L. The device with the longest channel corresponds to the most insignificant shift under CHCS, since the behavior of trapping-induced DIBL is suppressed by long channel device. This is because the potential variation due to electron trapping is growingly hard to extend to source side as channel length increases under Lin-Vth. Therefore, the Lin-Vth on long channel device has an insignificant degradation which is consistent with the model we supported. Consequently, the Lin-Vth shift on HfO2/TiN p-channel MOSFETs under CHCS results from electron trapping has been generalized in this work.

This letter studies the CHCS behaviors on HfO2/TiN p-channel MOSFETs. We found that the degradations result from electron trapping, leading Gm decrease and positive Lin-Vth shift, but Sat-$V_{th}$ shows an insignificant degradation during stress. This dissimilar behavior of $V_{th}$ is attributed to CHC-induced electron trapping induced DIBL. The devices with different channel length are introduced into evidence of trapping-induced DIBL behavior. As the result, the slightest Lin-Vth shift is corresponding to the HfO2/TiN p-channel MOSFET with the longest channel length.

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