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Fabrication of NiSi₂ nanocrystals embedded in SiO₂ with memory effect by oxidation of the amorphous Si/ Ni/ SiO₂ structure

P. H. Yeh
Department of Materials Science and Engineering, National Tsing Hua University, Hsin-Chu, Taiwan, Republic of China

H. H. Wu
Institute of Electronics of Electro-Optical Engineering, National Chiao Tung University, Hsin-Chu, Taiwan, Republic of China

C. H. Yu
Department of Materials Science and Engineering, National Tsing Hua University, Hsin-Chu, Taiwan, Republic of China

L. J. Chen
Department of Materials Science and Engineering, National Tsing Hua University, Hsin-Chu, Taiwan, Republic of China

P. T. Liu
Institute of Electronics of Electro-Optical Engineering, National Chiao Tung University, Hsin-Chu, Taiwan, Republic of China

C. H. Hsu
National Synchrotron Radiation Research Center, Hsin-Chu, Taiwan 300, Republic of China

T. C. Chang
Department of Physics and Institute of Electro-Optical Engineering, National Sun Yat-sen University, Kaohsiung, Taiwan, Republic of China and National Nano Device Laboratories, 1001-1 Ta-Hsueh Road, Hsin-Chu 300 Taiwan, Republic of China

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NiSi₂ nanocrystals embedded in the SiO₂ layer exhibiting a memory effect have been formed by dry oxidation of an amorphous Si/ Ni/ SiO₂ structure at 900 °C. A pronounced capacitance-voltage hysteresis was observed with a memory window of 1 V under the 2 V programming voltage for the samples. For dry oxidation at 800 °C, no distinct memory effect was detected. The processing of the structure is compatible with the current manufacturing technology of the semiconductor industry. The structure represents a viable candidate for low-power nanoscaled nonvolatile memory devices. © 2005 American Vacuum Society. [DOI: 10.1116/1.1913678]

I. INTRODUCTION

Recently, a memory-cell structure employing a semiconductor or metal nanocrystals as storage elements in metal-oxide-semiconductor (MOS) field transistors has received much attention as a promising candidate to replace a conventional dynamic random array memory or flash memories for future high-speed and low-power consumer memory devices.¹⁻⁵ Most studies have focused on the fabrication on Si and Ge nanocrystals in a MOS structure.⁶⁻¹⁴ The use of a floating gate composed of distributed nanocrystals reduces the problems of charge loss encountered in conventional floating-gate electrical erasable programmable read-only memory devices. It allows thinner tunnel oxide and, thereby, smaller operating voltages, better endurance and retention, and faster program/erase speed.⁷⁻⁹ The self-assembling of silicon or germanium nanocrystals embedded in SiO₂ layers has been widely investigated, and strong memory effects in MOS devices were reported.⁶⁻¹⁴ The metal nanocrystals’ memory has exhibited several advantages, such as stronger coupling with the conduction channel, a wide range of available work functions, higher density of states around the Fermi level, and smaller energy perturbation due to carrier confinement.³ The metal nanocrystals were usually fabricated by thermal annealing of the ultrathin metal film on the tunnel oxide.²⁻³ In the present study, NiSi₂ nanocrystals embedded in SiO₂ exhibiting memory effect were fabricated by oxidation of amorphous Si/ Ni/ SiO₂ structure.

II. EXPERIMENTAL PROCEDURES

Six-inch (100) oriented p-type silicon wafers were cleaned with standard RCA process, followed by a dry oxidation in an atmospheric pressure chemical vapor deposition furnace to form a 3 nm thick tunnel oxide. Subsequently, a 3.5 nm thick nickel layer was deposited onto the tunnel oxide by electron-beam evaporation. The nickel layer was capped by a 12.5 nm thick amorphous Si layer deposited also by sputtering. A schematic diagram of the structure is shown in Fig. 1(a). The stacked structure was, afterwards, dry oxidized for 10 min at 800 or 900 °C to form a layer with control oxide on the top. NiO or NiSi₂ nanocrystals were found to
precipitate and embed between tunnel oxide and control oxide, as depicted in Fig. 1(b). Finally, Al gate electrode was patterned and sintered, as illustrated in Fig. 1(c). The structural examinations were carried out in a transmission electron microscope (TEM) and synchrotron radiation facility using the x-ray absorption near-edge structure (XANES) analysis technique. The capacitance-voltage (C-V) measurements were performed by a precision LCR meter (HP 4284A) to study the electron charging and discharging effects of the NiSi₂ nanocrystals.

III. RESULTS AND DISCUSSION

Figure 2 shows typical bright-field, cross-sectional TEM images. In Fig. 2(a), a sample after 800 °C dry oxidation is shown. The nanocrystals were found to distribute in the control oxide randomly. However, for samples dry oxidized at 900 °C, as seen in Fig. 2(b), well-separated and spherical NiSi₂ nanocrystals embedded in the SiO₂ layer are observed. The top a-Si layer was completely oxidized to serve as the control oxide. Figure 3(a) shows the plan-view TEM image of a 900 °C oxidized sample. The mean size and aerial density of the NiSi₂ nanocrystals were measured to be about 8.5 nm and 2.5 × 10¹¹/cm², respectively. The size distribution of the nanocrystals is shown in Fig. 3(b). The nanocrystals were located between the tunnel oxide and the control oxide, without diffusing into the oxide. The characteristic is beneficial for the reliability and the yield of the memory device. The variation in morphology of these two samples with different oxidation temperatures is related to the rate of silicide formation. As the a-Si film was oxidized, oxygen may diffuse to the oxide/Si interface to form silicon oxide. If the NiSi₂ nanocrystals were already formed, they may move farther away from the oxide/Si interface. As a result, the selection of oxidation temperature and time are critical for forming nanocrystals. In growing SiO₂ film from Si, a film of SiO₂ with a thickness of $x_0$ consumes a layer of crystalline Si (c-Si) about 0.45$x_0$. Therefore, a Si substrate about 3.2 nm thick was oxidized to contribute to about a 7 nm thick SiO₂ in addition to the 3 nm thick tunnel oxide.

X-ray absorption near-edge structure analysis was used to determine the oxidation states of the samples. In XANES, a core electron is excited to higher bound or quasibound states, which contain information about coordination geometry and electronic aspects of the absorbing atom. Among most of the XANES studies, the standard materials with known valence are utilized as references, and compared with the unknown samples. Therefore, the measurements are frequently qualitatively analyzed, not quantitatively. The absorption edge of metallic Ni at 8 333 eV is marked in the figure by a vertical line to guide the eye. In the present study,
the Ni foil, NiO powder, and the epitaxial NiSi₂ layer on Si substrate were used as reference samples. As shown in Fig. 4(a), the edge position reflects zero-valence metal character of the as-deposited Ni layer. However, the local atomic structure seems to be quite disordered (like amorphous materials) so that the spectral features appear much less resolved as compared with those of Ni foils. For samples dry oxidized at 800 °C, substantial oxidation occurred, giving rise to many spectral features similar to what NiO exhibits, as shown in Fig. 4(b). This is attributed to the diffusion of nickel atoms into the a-Si film first, followed by oxidation. For the samples annealed at 900 °C, the features in its XANES spectrum look similar to those of NiSi₂, as shown in Fig. 4(c). It is thought that the formation of NiSi₂ and oxidation of a-Si film occurred first and the diffusion of Ni atoms was impeded.

Figure 5 shows the forward and reverse sweep C-V characteristics, indicating the electron charging and discharging effects of the nanocrystals embedded in SiO₂. The bidirectional C-V sweeps were performed from deep inversion to deep accumulation and in reverse, which exhibited an electron charging effect. As seen in Fig. 5(a), the C-V characteristic of the samples dry oxidized at 800 °C is rather poor. The hysteresis is clockwise, which is due to gate injection. It is correlated to the inactive NiO nanocrystals inside the control oxide, as seen in Fig. 2(a). The electron and the hole injections into the NiO nanocrystals are easier from the gate than from the Si substrate. If the oxidation temperature and time are well controlled, the memory effect can be improved. As shown in Fig. 5(b), for samples oxidized at 900 °C with the voltage swept from 2 to (−8) V and back to 2 V, an outstanding threshold voltage shift of 1 V is observed. As the whisked voltages were increased to 5 and 8 V, more obvious C-V shifts of 8 and 13 V respectively, are seen. It is perceived that the hysteresis is counterclockwise, which is due to injection of electrons from the deep inversion layer and injection of holes from the deep accumulation layer of Si substrate. The result of the C-V shift indicates that the charging effects of NiSi₂ nanocrystals are more significant than those of the semiconductor nanocrystals. In Fig. 6, the threshold voltage shift opens with increasing the gate voltage for the samples oxidized at 900 °C. For the samples oxidized at 800 °C, the significant memory window is lacking. The TEM images and the C-V characteristics indicate that the
nickel diffusion can be alleviated by increasing the process temperature. The memory effect of the samples with a process temperature of 1000 °C was found to be rather poor, possibly due to the agglomeration of NiSi2 at a temperature above the eutectic temperature (993 °C) for Ni-Si system.

Figure 7(a) shows the band diagrams with different gate polarities of the memory device for the samples oxidized at (a) 800 °C and (b) 900 °C with “write” and “erase” operations.

Figure 7(b) illustrates how the device works for samples dry oxidized at 900 °C, as follows: When the device is written or programmed, the electrons tunnel directly from the Si substrate through the tunnel oxide, and are trapped in the NiSi2 nanocrystals. On the other hand, when the device is erased, the electrons may tunnel back to the deep accumulation layer of Si substrate. The control oxide is utilized to prevent the carriers of gate electrode from injecting into the NiSi2 nanocrystals by Fowler-Nordheim tunneling.

The most important advantage using the metal nanocrystals over their semiconductor counterparts is that the metal nanocrystals do not bear a voltage drop from gate voltage.
which means all the voltages provided from control gate are dropped to tunnel oxide and control oxide. The operating voltage of the memory devices with conventional floating gate or semiconductor nanocrystals embedded in SiO₂ is above 7 or 5 V. In our approach to fabricate the NiSi₂ nanocrystals embedded in SiO₂ by dry oxidation, a lower aerial density of NiSi₂ nanocrystals were measured to be 8.5 × 10¹¹/cm², respectively. A significant C-V hysteresis of voltage shift of 1 V was observed. The advantages of the method are that it is simple and well controlled. The implementation of the present structure is compatible with the current manufacturing technology of semiconductor industry and represents a viable candidate for low-power nanoscaled nonvolatile memory devices.

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![Graph showing C-V hysteresis loops for samples heated at 150 °C for up to 10 h.](image)

IV. CONCLUSIONS

NiSi₂ nanocrystals embedded in SiO₂ have been fabricated with appropriate control of the process temperature and time. In samples dry oxidized at 900 °C, the mean size and aerial density of NiSi₂ nanocrystals were measured to be 8.5 nm and 2.5 × 10¹¹/cm², respectively. A significant C-V hysteresis of voltage shift of 1 V was observed. The implementation of the present structure is compatible with the current manufacturing technology of semiconductor industry and represents a viable candidate for low-power nanoscaled nonvolatile memory devices.