Comments and Corrections

Correction to “A Third-Order ΣΔ Modulator in 0.18-μm CMOS With Calibrated Mixed-Mode Integrators”

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We recently received feedback from the authors of [2] that the modulator structure in Fig. 1(c) used in our recent paper [1] is similar to that described in [2]. This paper should have been included as a reference in our paper [1]. It was left out by oversight.

REFERENCES

Correction to “A 15-Bit 40-MS/s CMOS Pipelined Analog-to-Digital Converter With Digital Background Calibration”

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In the above paper [1], the authors commented that the gain error correction plus the DAC noise cancellation (GEC + DNC) technique can only be applied to multibit pipeline stages and it also doubles the required opamp’s output range [2]–[5]. This statement is misleading and partially incorrect, as pointed out by the author of [2]. The authors would like to change the comment as follows:

If a pipeline stage includes a multibit sub-DAC, the mismatch errors in the sub-DAC can be eliminated by the DAC noise cancellation technique [2]. Correcting the pipeline stage’s gain error can further improve the A/D resolution [3]–[5]. The gain error correction technique of [3] demands an increase of the required opamp’s output range and an increase of complexity in the sub-DAC design [4]. In the [4] case, the required opamp’s output range is increased by 50%. While the continuous gain correction technique of [5] does not increase the required opamp’s output range, its performance depends on the accuracy of the sub-ADC [4], and it cannot function properly under certain input conditions.

REFERENCES