
Electrical Enhancement of Solid Phase Crystallized Poly-Si Thin-Film Transistors with Fluorine Ion Implantation

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Solid phase recrystallized polycrystalline silicon thin-film transistors (SPC poly-Si TFTs) with fluorine ion implantation were investigated in this study. Electrical characteristics and reliability of the proposed poly-Si TFTs were improved effectively, especially for field effect mobility and off current. The fluorine-ion-implanted poly-Si TFT can suppress the hot carrier multiplication near the drain side, leading to superior endurance to electrical stress compared with conventional poly-Si TFTs. It was found that fluorine ions will pile up at the poly-Si interface during thermal annealing, without the initial deposition of pad oxide. The proposed technology is manageable and compatible with conventional poly-Si TFT fabrication. As the ion dosages increase more than $5 \times 10^{15} \text{cm}^{-2}$, however, the electrical characteristics of poly-Si TFTs were degraded due to the increase of trap state density caused by the fluorine segregation in the poly-Si film.

In recent years polycrystalline silicon thin-film transistors (poly-Si TFTs) have been widely used in many applications, especially for active matrix liquid phase displays (AMLCDs). The major attraction of the poly-Si TFTs in AMLCDs lies in the greatly improved carrier mobility. In addition, the capabilities of integrating the pixel switching elements, pixel array, and peripheral driving circuit on the same substrates are also attractive. Application of the poly-Si TFTs enables the fabrication of peripheral circuit and TFT array on the same glass substrate. The process complexity can be greatly simplified and the cost also can be reduced. TFT arrays with high density, high resolution, and high aperture ratio can be realized by using poly-Si TFTs as pixel switching elements. The channel width of poly-Si TFT devices can be scaled down while meeting the same pixel driving requirements as in a-Si TFT AMLCDs. For making high-performance poly-Si TFTs, low-temperature technology is required for the realization of commercial flat-panel displays (FPDs) on inexpensive glass substrate, because the maximum process temperature is limited to less than 600°C. The solid phase crystallization (SPC) process is widely used to recrystallize Si film due to its low cost and high uniformity in grain size. However, the SPC process, requiring 24–48 h, is a time-consuming procedure, which obviously affects the throughput and thermal budget of fabrication processes. Besides, the lower field effect mobility ($\mu_{FE}$) limits the development for SPC poly-Si TFTs, and the poly-Si TFTs suffer from undesirable leakage current from trap states at the grain boundaries. Based on these issues of poly-Si TFTs, several processes have been applied to reduce the trap states and enhance the electrical characteristics. Hydrogen plasma treatment is a widely used method to passivate the trap states to avoid undesirable leakage current, but it is difficult to control the hydrogen concentration in the poly-Si film. Recently, fluorine ion implantation has been applied to improve the electrical characteristics by eliminating the defects in the grain boundary. The main purpose for fluorine ion implantation is to passivate the undesirable strain bonds at the interface between poly-Si and SiO$_2$. It was found that the fluorine piled up at the interface between the poly-Si and the oxide, eliminating the strain bonds, and can be the terminators of dangling bonding in poly-Si. In addition, the stronger Si–F bonds can replace weaker Si–H and Si–Si bonds and exhibit superior electrical reliability against dc stress, compared to standard poly-Si TFT counterparts. However, previous reports indicate the need for an additional oxide layer deposition and an additional thermal annealing. These extra steps will increase the difficulty for fabrication of the poly-Si TFTs.

In this work the electrical behavior of SPC fluorine-ion-implanted poly-Si TFTs was investigated comprehensively. The a-Si layer was deposited by using a low-pressure chemical vapor deposition (LPCVD) system. In addition, a simple recrystallization process was performed without the need of an initial pad oxide deposition, in contrast to the prior art.

**Experimental**

A 50 nm thick, undoped a-Si layer was deposited on an oxide-coated silicon wafer by a LPCVD system. Then the fluorine ions were implanted into the a-Si layer without initial deposition of the pad oxide layer. The implantation conditions were ion accelerating energy 11 keV and the dosages $5 \times 10^{13}$, $5 \times 10^{14}$, and $5 \times 10^{15}$ cm$^{-2}$, respectively. The recrystallization process for the amorphous silicon (a-Si) film, with and without fluorine ion implantation, is performed by a thermal furnace at 600°C for 24 h in N$_2$ ambient. After patterning the Si active regions, a 50 nm thick tetra-ethylorthosilicate (TEOS) layer and a 200 nm thick poly-Si film were deposited on the substrate. The poly-Si film was crystallized by a heat treatment at 600°C for 24 h. The fluorine-ion-implanted poly-Si TFT was fabricated by conventional photolithography and etching processes. The poly-Si films were recrystallized by a thermal annealing process at 600°C for 24 h.

**Figure 1.** The cross section of F-ion incorporated poly-Si TFT structure.
The decrease of the fluorine-implanted poly-Si TFT is higher than $53.82 \text{ cm}^2/\text{V}$. Drain current ($I_D$)/threshold voltage ($V_{TH}$) benefits the proposed poly-Si TFT application. The poly-Si TFTs is significantly enhanced. The on characteristics are improved with a fluorine implantation dosage $5 \times 10^{13}$ cm$^{-2}$. Figure 3 illustrates the transfer characteristics of poly-Si TFT with fluorine ion implantation at an ion dosage of $5 \times 10^{13}$ cm$^{-2}$ and a typical poly-Si TFT. Figure 2 summarizes major electrical parameters of the poly-Si TFT devices. The threshold voltage ($V_{TH}$) is given by the gate voltage which yields the drain current ($I_D$) ($I_{DS} = 10 \text{nA} \times W/L$). The electrical characteristics are improved with a fluorine implantation dosage $5 \times 10^{13}$ cm$^{-2}$, especially for the $\mu_{FE}$ and $V_{TH}$. The value of $\mu_{FE}$ for the fluorine-implanted poly-Si TFT is higher than $53.82 \text{ cm}^2/\text{V}$. The decrease of $V_{TH}$ benefits the proposed poly-Si TFT application on electronics. Also, the on current of the fluorine-incorporated poly-Si TFTs is significantly enhanced. The $I_D-V_{TH}$ output characteristic is shown in Fig. 3, exhibiting the great improvement at a drain current of the fluorine-ion-implanted poly-Si TFTs at $V_G = 4$, 7, and 10 V, respectively. Figure 4 shows the activation energy ($E_A$) of drain current as a function of gate voltage measured at $V_D = 5$ V for the standard and the fluorine-implanted poly-Si TFTs. $E_A$ was obtained by the measurement of $I_D-V_G$ characteristics at temperatures ranging from 20 to 150°C. $E_A$ represents the carrier transportability, which is related to the barrier height in the poly-Si channel. The $E_A$ of off-state current is increased and the $E_A$ of on-state current is reduced for the fluorine-ion-implanted poly-Si TFT, implying that fluorine implantation alters the trap state density. The fluorine ions effectively piled up at the poly-Si interface without pad oxide deposition, as demonstrated in Fig. 5, the secondary ion mass spectroscopic (SIMS) analysis. The ostensibly oxidized Si layer supplies fluorine ions a driving force to segregate at the surface during thermal processes. Hence, no extra thermal annealing steps were needed to segregate fluorine ions at the surface as compared with prior reports. It has been reported that the deep trap states can be eliminated effectively by using fluorine ion implantation, leading to the reduced $V_{TH}$ in n-channel poly-Si TFTs. In this work, a minimum of $V_{TH}$ is obtained with an optimal fluorine ion implantation dosage of $5 \times 10^{13}$ cm$^{-2}$. To investigate device reliability, the poly-Si TFTs were biased stressed at $V_D = 20$ V and $V_G = 20$ V for varied time durations of 100, 200, 600, and 1000 s. More moderate threshold voltage variation ($\Delta V_{TH}$) was obtained in the fluorine-ion-implanted poly-Si.
TFTs than that in the standard poly-Si TFTs, as shown in Fig. 6. Hot carrier multiplication near the drain side causes the degradation of $V_{TH}$, $I_{ON}$, and subthreshold swing ($S.S.$). It has been reported that the hot-carrier-stress-induced degradation is attributed to the following two possible cases: the generation of gate oxide/poly-Si interface states and formation of Si–Si or Si–H weak bonds in the poly-Si channel. The fluorine ions terminate the Si dangling bonds, and the stronger Si–F bonding possesses superior endurance against hot carrier stress, thereby exhibiting enhanced reliability. Figures 7 and 8 separately show the $\Delta I_{ON}$ and $\Delta S.S.$ of poly-Si TFTs after dc bias stress. Because the strong Si–F bonds prevent the generation of Si dangling bonds, the fluorine-ion-implanted poly-Si TFT can suffer less degradation of $V_{TH}$, $I_{ON}$, and $S.S.$ compared to the conventional poly-Si TFT.

Electrical properties of the fluorine-ion-implanted poly-Si TFT with heavy implantation dosages were also studied in this work. Figure 9 shows the electrical properties of poly-Si TFTs with various fluorine ion implantation dosages. Table I summarizes the key electrical parameters. It is found that the electrical characteristics of ploy-Si TFT are degraded as the implantation dosage increases, especially for the case of $5 \times 10^{13}$ cm$^{-2}$. The $I_{ON}$, $V_{TH}$, and $S.S.$ are all degraded for higher fluorine ion implantation dosage, as compared to the standard poly-Si TFT. With the fluorine implantation dosages higher than Si solid solubility, the trap state density could be increased significantly as the implantation dosage increases. The segregated fluorine ions in the poly-Si channel will not passivate the trap states but generate additional defects to degrade the electrical properties. In addition, the fluorine ions are prone to accumulate and form more fluorine clusters during the sequent fabrication process, even worsening the electrical characteristics.

It is thought that one of the possible causes for the electrical improvement of the poly-Si TFTs might be from the enhancement in the recrystallized poly-Si grain size after ion implantation. However, the possibility does not appear in this work. The SEM image shown in Fig. 10 apparently reveals a little difference in grain size between the poly-Si film with and without fluorine ion implantation. Therefore, it is reasonable to believe that the electrical characteristics of the fluorine-ion-implanted poly-Si TFTs are less dependent on the poly-Si grain size. We conclude that the incorporation of fluorine in poly-Si film plays a critical role in the electrical improvement of the fluorine-ion-implanted poly-Si TFT.

**Conclusion**

In this work it has been found that electrical characteristics of the poly-Si TFT are enhanced greatly with an optimum implantation dose of $5 \times 10^{13}$ cm$^{-2}$ by decreasing the trap state density. Significant improvements in field effect mobility and electrical reliability have been obtained, presumably due to the formation of stronger Si–F bonds instead of weak Si–Si and Si–H bonds in the poly-Si layer. The F-incorporated poly-Si TFTs thereby can possess higher hot carrier endurance and improve device reliability. With the fluorine implantation dosages higher than Si solid solubility, the trap state density could be increased significantly as the implantation dosage increases. The segregated fluorine ions in the poly-Si channel do not passivate the trap states but generate additional defects to degrade the electrical properties. The proposed technology with...
fluorine ion implantation in poly-Si is practical and compatible with the conventional poly-Si TFT processes, potentially applicable for AMLCDs.

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References


Table I. Critical electrical parameters for the standard and the F-ion-implanted poly-Si TFTs with various implantation dosages.

<table>
<thead>
<tr>
<th>μFE (cm²/V s)</th>
<th>VTH (V)</th>
<th>S.S. (V/dec)</th>
<th>ION/IOFF (10⁶)</th>
<th>Nt (10¹² cm⁻²)</th>
</tr>
</thead>
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<tr>
<td>Standard</td>
<td>19.74</td>
<td>6.24</td>
<td>1.20</td>
<td>26.01</td>
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<tr>
<td>F dose 5x10¹⁳ cm⁻²</td>
<td>54.48</td>
<td>4.78</td>
<td>0.97</td>
<td>87.62</td>
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<tr>
<td>F dose 5x10¹⁴ cm⁻²</td>
<td>48.12</td>
<td>6.69</td>
<td>1.13</td>
<td>67.31</td>
</tr>
<tr>
<td>F dose 5x10¹⁵ cm⁻²</td>
<td>15.17</td>
<td>10.36</td>
<td>1.62</td>
<td>1.94</td>
</tr>
</tbody>
</table>

Figure 10. SEM image of the poly-Si film, with and without fluorine ion implantation.