A New Extraction Algorithm for the Metallurgical Channel Length of Conventional and LDD MOSFET's

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Abstract—A new extraction algorithm for the metallurgical channel length of conventional and LDD MOSFET's is presented, which is based on the well-known resistance method with performing a special technique to eliminate the uncertainty of the channel length as well as to reduce the influence of the parasitic source/drain resistance on threshold-voltage determination. In particular, the metallurgical channel length is determined from a wide range of gate-voltage-dependent effective channel length at an adequate gate overdrive. The 2-D numerical analysis clearly show that the adequate gate overdrive is strongly dependent on the dopant concentration in the source/drain region. Therefore, an analytic equation is derived to determine the adequate gate overdrive for various source/drain and channel doping. It shows that higher and lower gate overdrives are needed to accurately determine the metallurgical channel length of conventional and LDD MOSFET devices, respectively. It is the first time that we can give a correct gate overdrive to extract \( L_{\text{met}} \) not only for conventional devices but also for LDD MOS devices. Besides, the parasitic source/drain resistance can also be extracted using our new extraction algorithm.

I. INTRODUCTION

The channel length is one of the most important parameters for MOSFET's. In addition to performance analysis and fabrication process control, the channel length plays a major role on device design and circuit simulation. The so-called channel length has two different definitions in literatures. One is the effective channel length \( (L_{\text{eff}}) \), which represents the 'effective' channel region that can be strongly modulated by the gate bias, while the metallurgical channel length \( (L_{\text{met}}) \) is defined to be the distance between the metallurgical junctions of source and drain diffusions in the channel surface of a MOSFET, as illustrated in Fig. 1(a).

The extraction algorithms for effective channel length proposed in literatures were usually based on the resistance \([1]-[8]\) and capacitance \([9], [10]\) measurements. In addition to the problems of parasitic capacitance, equipment with high resolution is required to measure the small intrinsic gate capacitance down to the order of femto farads. Therefore, the capacitance method is impractical for applications. Comparing with the capacitance methods, the extraction algorithms based on the resistance methods are much simpler. Based on the resistance measurements, the methods \([1], [2], [4]\) determined \( L_{\text{eff}} \) in a high gate overdrive range, which are applicable for conventional MOSFETs; while the method presented in \([8]\) used a low gate overdrive range for LDD MOSFET's. There is no definite method to determine the magnitude of gate overdrive.

In this paper, an analytic equation is derived to predict the correct gate overdrive in order to determine the unique \( L_{\text{met}} \) from the extracted \( L_{\text{eff}} \) for both conventional and LDD MOSFET's. In Section II, a new extraction algorithm for the metallurgical channel length of MOSFET's is described. Our extraction algorithm is based on the resistance method, which from which we can determine the effective channel-length reduction \( (\Delta L_{\text{eff}}) \). According to our analysis, the metallurgical channel-length reduction \( (\Delta L_{\text{met}}) \) can be determined from a wide range of gate-bias dependent \( \Delta L_{\text{eff}} \). To improve the accuracy, the threshold-voltage correction is performed iteratively. In Section III, the 2-D numerical analysis shows that the major deviation in \( \Delta L_{\text{met}} \) extraction arises from the nonideal resistance distribution due to carrier redistribution. In addition, an analytic model is proposed to evaluate this phenomenon, and comparisons between 2-D numerical
analysis and analytic model evaluation are performed. The proposed extraction algorithm is verified by comparing the extraction results from 2-D simulation and experimental devices in Section IV. Finally, conclusions are given in Section V.

II. DESCRIPTIONS OF THE EXTRACTION ALGORITHM

For an ideal MOSFET device operated in the linear (low drain bias) region, the drain current can be expressed as

\[ I_D = \frac{\mu C_{ox} W_{eff}}{L_{eff}} \left(V_{gs} - \frac{V_D}{2}\right) V_D \]  

where \( \mu \) is the effective channel mobility, which is a function of applied gate bias; \( C_{ox} \) is the gate oxide capacitance per unit area; \( W_{eff} \) and \( L_{eff} \) are the effective channel width and length, respectively; \( V_{gs} \) and \( V_D \) are the intrinsic gate to source and drain to source voltage drops, as shown in Fig. 1(b); and \( V_T \) is the threshold voltage. If the total parasitic source/drain resistance is \( R_P \) and the source and drain are symmetrical, then we have \( V_{gs} = V_G - \frac{V_D}{2} R_P / \frac{1}{2} \) and \( V_D = V_D S - \frac{1}{2} R_P \), where \( V_D S \) is equal to \( I_{ds} \). Substituting \( V_{gs} \) and \( V_D \) into (1), then the total resistance \( R_T \) is given by

\[ R_T = R_P + R_{ch} = R_P + \frac{L_M - \Delta L_{eff}}{\mu C_{ox} W_{eff} \left(V_G - \frac{V_D}{2}\right)} \]  

where \( R_{ch} \) is the channel resistance; \( L_M \) is the mask channel length; and \( \Delta L_{eff} \) is the difference between mask channel length and effective channel length. If \( \Delta L_{eff} \) is assumed to be the same for all test devices in a testkey and the threshold voltage of all test devices are known exactly, we can determine \( \Delta L_{eff} \) from (2) by the following steps:

1) Taking the \( R_T \) value versus \( L_M \) at the same gate overdrive for all devices, the slope \( (S_{lopo}) \) and the intercept in y-axis \( (Y_{cept}) \) can be obtained by a least squares fitting as follow

\[ S_{lopo} = \left[ \frac{\mu C_{ox} W_{eff}}{L_{eff}} \left(V_G - \frac{V_D}{2}\right) \right]^{-1} \]  

\[ Y_{cept} = R_P - S_{lopo} \times \Delta L_{eff} \]  

2) Varying the gate overdrive, we can get the variations of \( Y_{cept} \) with respect to \( S_{lopo} \).

3) Differentiating \( Y_{cept} \) in (4) by \( S_{lopo} \), we have

\[ \Delta L_{eff} = \frac{dY_{cept}}{dS_{lopo}} \]  

Note that each \( \Delta L_{eff} \) at a given gate overdrive is deduced by its small gate overdrive interval, which is a constant within this small gate overdrive interval. Moreover, the extraction procedure described above needs to accurately determine the threshold voltages for all devices with different channel lengths. Similarly, the effective channel mobility and the parasitic source/drain resistance are assumed to be constant within a small gate overdrive interval for all mask channel lengths. The extracted overall effective channel-length reduction \( (\Delta L_{eff}) \) in (5) is gate-bias dependent [1], [2], [5], [6], and the determination of the metallurgical channel-length reduction from the gate-bias dependent effective channel-length reduction will be the major emphasis of this paper.

There are two basic guides to determine \( \Delta L_{met} \) from the gate-bias dependent \( \Delta L_{eff} \): (a) For conventional MOSFET devices, \( \Delta L_{eff} \) is chosen at higher gate overdrive [1]; (b) For LDD (lightly doped source/drain) MOSFET devices, \( \Delta L_{eff} \) is chosen at lower gate overdrive [8]. The major reasons for using these two guides will be described in details in the next section. Once \( \Delta L_{met} \) has been determined, the parasitic source/drain resistance \( (R_P) \) can be derived. \( R_P \) can be determined from (2) and is the value of \( R_T \) when \( L_M \) is equal to \( \Delta L_{met} \). Therefore, the definition of \( R_P \) is the total resistance outside the metallurgical junctions of source and drain diffusions. As mentioned above, for each gate overdrive there is a different \( R_P \) because \( R_P \) is gate-bias dependent. Nevertheless, the key step in channel-length extraction is to accurately determine the threshold voltage of each device so that \( R_T \) can be evaluated at the same gate overdrive [7], [8]. With the improperly deduced threshold voltage, the extracted \( \Delta L_{eff} \) will be far away from its exact value. Consequently, the threshold voltage must be determined accurately and carefully.

In our extraction method, the normalized current method is used to determine the threshold voltage. First, the longest channel-length device is chosen to ensure negligible short-channel and parasitic source/drain resistance effects; and its threshold voltage is determined by the conventional maximum transconductance extrapolation method. The current at the extracted threshold voltage divided by the channel length is defined as the ‘normalized current’. Next, this ‘normalized current’ multiplied by other shorter channel length is used to determine the threshold voltage of shorter device. However, the channel length of shorter device before determining its threshold voltage is unknown except that the mask channel length is known. Therefore, initially the mask length is used instead of the channel length. This is a good approximation in the case of \( L_M \gg \Delta L_{met} \) and will produce serious errors for small \( L_M \). In addition, it is known that the parasitic source/drain resistance \( R_P \) may greatly reduce the drain current of short channel devices. To reduce the influence of \( \Delta L_{met} \) and \( R_P \) on the threshold-voltage determination, the ‘iteration’ method proposed in [8] is used. After extracting \( \Delta L_{met} \) and \( R_P \), from (2) we have

\[ I_{DS} \left( \frac{V_D S}{R_T - R_P} \right) = \frac{\mu C_{ox} W_{eff} \left(V_G - \frac{V_D}{2}\right) V_D S}{L_{met}} \]  

where \( I_{DS} \) is the intrinsic drain current, which does not include the \( R_P \) effect. Therefore, we can determine \( V_T \) from the extracted \( \Delta L_{met} \) and (6), and further to extract \( \Delta L_{met} \). This process is repeated until the extracted \( V_T \) and \( \Delta L_{met} \) self-consistently converge to their true values, as expressed by a flowchart shown in Fig. 2.

III. NUMERICAL ANALYSIS AND ANALYTIC MODEL EVALUATION

A. Numerical Analysis

In the previous section, we have assumed that the MOS devices exhibit the ideal characteristics. The ideal resistance distribution is shown in Fig. 3 by the dashed line, in which
the $x$-axis is the distance along the channel $x$(µm), and the $y$-axis is the channel resistance per unit length $dR/dx$(Ω/µm) computed by evaluating the change of the electron quasi-Fermi-level over a small interval divided by the distance and source-drain current [5]. Note that the area under the curve shown in Fig. 3 represents the resistance of a MOSFET. For an ideal device, the parasitic source/drain resistance (the resistance outside the $L_{\text{met}}$ region) is a fixed value and is independent of gate overdrive, whereas the channel resistance (the resistance in the $L_{\text{met}}$ region) is proportional to the metallurgical channel length $L_{\text{met}}$ and is bias-dependent. The maximum $dR/dx$ (signed $S_{\text{max}}$) must be the same for all channel lengths at a given gate overdrive. This means that the deduced threshold voltage is accurate, i.e., all devices are operated at the same gate overdrive. From the ideal devices shown in Fig. 3, the total resistance can be expressed as

$$R_T = R_P + S_{\text{max}} \times (L_M - \Delta L_{\text{met}})$$

(7)

where $R_P = 2R_{\text{co}} + 2R_n$; $R_{\text{co}}$ is the contact resistance, which is not shown in Fig. 3; $R_n$ is the resistance between source/drain contact and channel region, as shown in Fig. 3. In general, $R_{\text{co}}$ is constant, while $R_n$ is bias-dependent. Nevertheless, $R_{\text{co}}$ and $R_n$ are all constants for the ideal characteristics. Now, $S_{\text{loge}}$ and $Y_{\text{cept}}$ in (5) can be obtained from (7): $S_{\text{loge}} = S_{\text{max}}$ and $Y_{\text{cept}} = R_P - S_{\text{max}} \times \Delta L_{\text{met}}$. According to (5), the channel-length reduction can be obtained by

$$\Delta L_e = -\frac{d}{dS_{\text{max}}}(R_P - S_{\text{max}} \times \Delta L_{\text{met}})$$

(8)

where $\Delta L_e$ is the extracted channel-length reduction. Note that the subscript in $\Delta L_e$ is used to distinguish the exact (given) $\Delta L_{\text{met}}$ value. If $R_P$ is independent of bias condition (assumption for ideal MOSFETs), $\Delta L_e$ will be exactly equal to $\Delta L_{\text{met}}$.

However, for a practical MOSFET, the total resistance cannot be simply expressed by (7), and the reasons are shown in Fig. 3. It’s clearly seen that the real $dR/dx$ is not the same as that of an ideal device, so the channel resistance $R_{\text{ch}}$ is less than $S_{\text{max}} \times (L_M - \Delta L_{\text{met}})$ and can be represented by

$$R_{\text{ch}} = S_{\text{max}} \times (L_M - \Delta L_{\text{met}}) - R_{c1} - R_{c2}$$

(9)

where $R_{c1}$ and $R_{c2}$ are the areas indicated in Fig. 3 and are bias-dependent, which represent the difference of channel resistance between ideal and practical MOSFET’s. On the other hand, the $R_n$ in the parasitic resistance $R_P$ is also dependent on gate overdrive for a practical device. Now, the total resistance of a practical MOSFET in (7) can be rewritten as

$$R_T = 2R_{\text{co}} + A + S_{\text{max}} \times (L_M - \Delta L_{\text{met}})$$

(10)

where $A = 2R_n - R_{c1} - R_{c2}$. From (10), $Y_{\text{cept}}$ becomes

$$Y_{\text{cept}} = 2R_{\text{co}} + A - S_{\text{max}} \times \Delta L_{\text{met}}.$$  

(11)

Applying (5), the extracted channel-length reduction becomes

$$\Delta L_e = \Delta L_{\text{met}} - \frac{dA}{dS_{\text{max}}}.$$  

(12)

In practice, (12) is the effective channel-length reduction $\Delta L_{\text{eff}}$ as mentioned in the previous section. This equation described the relation between the extracted $\Delta L_{\text{eff}}$ and the real $\Delta L_{\text{met}}$. If $dA/dS_{\text{max}}$ in (12) is equal to zero, the extracted $\Delta L_{\text{eff}}$ will be equal to $\Delta L_{\text{met}}$. It is worth noting that $\Delta L_{\text{met}}$ in (11) and (12) is a constant, while $\Delta L_e$ and $dA/dS_{\text{max}}$ are bias-dependent. The resistances $R_n$, $R_{c1}$ and $R_{c2}$ are all bias-dependent. Anyway, $R_n$, $R_{c1}$ and $R_{c2}$ cannot be extracted from the extraction algorithm as described in Section II. Therefore, we compute these resistances from
a 2-D device simulator-SUMMOS [11], as demonstrated in Fig. 4(a). In this figure, $\Delta L_{\text{eff}}, dA/dS_{\text{max}}, 2dR_{n}/dS_{\text{max}}$ and $-(dR_{c1} + dR_{c2})/dS_{\text{max}}$ are computed as a function of $V_{GS} - V_{T}$ and the given $L_{\text{met}}$ is 0.2 $\mu$m. Note that $\Delta L_{\text{eff}}$ in Fig. 4 is calculated by (5), where $S_{\text{max}}$ is obtained from Fig. 3, $Y_{\text{cept}}$ is calculated by $R_{T} - S_{\text{max}}L_{M}$. As mentioned above, $\Delta L_{\text{eff}}$ is bias-dependent and its value decreases from 0.5 $\mu$m to 0.1 $\mu$m when $V_{GS} - V_{T}$ increases from 0 to 5 V. Similarly, $dA/dS_{\text{max}}$ increases from negative to 0.1 $\mu$m. If we add $\Delta L_{\text{eff}}$ and $dA/dS_{\text{max}}$ together, the sum is nearly a constant, i.e., 0.2 $\mu$m, just the given value for $L_{\text{met}}$. In other words, when $dA/dS_{\text{max}}$ is equal to zero, $\Delta L_{\text{eff}}$ is exactly equal to $\Delta L_{\text{met}}$, and this situation happens at a gate bias of $V_{GS} - V_{T} = 1.8$ V, as shown in Fig. 4(a). This means that the decrease rate of $R_{c1}$ + $R_{c2}$ is just compensated by the decrease rate of $2R_{n}$.

Note that Figs. 3 and 4(a) are for LDD MOSFET’s. For a conventional device, as shown in Fig. 5, it is clearly shown that $R_{n}$ is nearly equal to zero because of the heavily doped source/drain region, so its gate modulation $2dR_{n}/dS_{\text{max}}$ in Fig. 4(b) approaches to zero. On the other hand, $R_{c1}$ and $R_{c2}$ are similar for conventional and LDD MOSFET’s. Hence, the curve of $-(dR_{c1} + dR_{c2})/dS_{\text{max}}$ in Fig. 4(b) is similar to that in Fig. 4(a). Again, the sum of $dA/dS_{\text{max}}$ and $\Delta L_{\text{eff}}$ is a constant. Apparent differences shown in this figure are $\Delta L_{\text{met}}$ and $dA/dS_{\text{max}}$; unlike the LDD MOSFET’s, $\Delta L_{\text{eff}}$ and $dA/dS_{\text{max}}$ approach to 0.2 and 0 $\mu$m at higher gate overdrive, respectively.

From the 2-D numerical analysis for LDD and conventional MOSFET’s mentioned above, the principle to choose $L_{\text{met}}$ from $L_{\text{eff}}$ as described in the previous section has been given.

B. Analytic Model Evaluation

The resistance distribution of a typical MOSFET can be divided into 7 components, as shown in Fig. 6. They are:

1. Gate-controlled channel resistance,
2. Carrier diffusion related channel resistance,
3. Carrier diffusion related source/drain resistance,
4. Gate overlapped source/drain resistance,
5. Gate fringe field induced resistance,
6. Source/drain sheet resistance,
7. Contact resistance (not shown in Fig. 6).

The gate-controlled channel resistance locates at the center of the channel and is strongly modulated by the gate voltage. Components 2 and 3 come from carrier redistribution between source/drain region and channel region. Higher carrier concentration in source/drain region will diffuse to channel region where the carrier concentration is lower. This carrier redistribution decreases the channel resistance and increases the source/drain region resistance. Therefore, Component 2 is smaller than Component 1, while Component 3 is larger than Component 4, as shown in Fig. 6. Components 4 and 5 are also modulated by gate bias, which are weak and very weak functions of gate bias, respectively. Component 6 is related to source/drain doping concentration and Component 7 is constant.
Note that \( dA/dS_{\text{max}} \) is an indicator of how \( \Delta L_{\text{eff}} \) approaches to \( \Delta L_{\text{met}} \). As the value \( dA/dS_{\text{max}} \) approaches to zero, \( \Delta L_{\text{eff}} \) approaches to \( \Delta L_{\text{met}} \). Here, \( S_{\text{max}} \) is a strong function of gate bias (Component 1), and \( A \) is related to Components 2, 3, 4, 5 and 6. However, Component 6 is independent of gate bias and Component 5 is a very weak function of gate bias, so we can neglect them. Component 4 is basically a weak function of gate bias. For modern MOSFET devices, \( \Delta L_{\text{met}} \) is small and, therefore, the overlapped region is further smaller than it. Again, Component 4 is abandoned. Now, we only consider Components 1, 2 and 3 to compute \( dA/dS_{\text{max}} \).

For a small drain to source voltage (e.g., \( V_{DS} = 0.05 \) V), the shape of Fig. 5 is nearly symmetrical, i.e., \( R_{c1} \approx R_{c2} \). Therefore, \( dA/dS_{\text{max}} \) becomes

\[
\frac{dA}{dS_{\text{max}}} = \frac{d}{dS_{\text{max}}}(2R_n - R_{c1} - R_{c2})
\]

\[
= \frac{d}{dS_{\text{max}}}(2R_n - 2R_{c1}).
\]

(13)

where \( R_n \) and \( R_{c1} \) can be approximated by the triangle areas shown in Fig. 5 and are given by \( R_{c1} = W_p(S_{\text{max}} - S_{\text{jun}})/2 \) and \( R_n = W_n S_{\text{jun}}/2 \), in which \( W_p \) and \( W_n \) are the widths of carrier redistribution in the channel and source/drain regions, respectively; \( S_{\text{jun}} \) is the value of \( dR/dx \) at the metallurgical junction. Now, (13) becomes

\[
\frac{dA}{dS_{\text{max}}} = \frac{d}{dS_{\text{max}}} [(W_p + W_n) S_{\text{jun}} - W_p S_{\text{max}}].
\]

(14)

The exact values for \( W_p \) and \( W_n \) can be obtained by solving the current density and Poisson’s equations. To simplify the problem, we consider that \( W_p \) and \( W_n \) are proportional to Debye length in this paper. Since the majority-carrier concentration deviated from the dopant concentration is governed by the extrinsic Debye length \( L_D \) [12], which is expressed by

\[
L_D = \left[ \frac{q^2 kT}{2\pi e (n+p)} \right]^{1/2}.
\]

Therefore, \( W_p \) and \( W_n \) can be expressed as

\[
W_p = k_1 L_D \approx k_2 [C_{ox}(V_{GS} - V_T)/Y]^{-\frac{1}{2}},
\]

(15)

\[
W_n = k_1 L_D \approx k_2 [qN_D + C_{ox}(V_{GS} - V_{FBn})/Y]^{-\frac{1}{2}}
\]

(16)

where \( k_1 \) and \( k_2 \) are the constants; \( L_{DP} \) and \( L_{Dy} \) are the extrinsic Debye length in the channel and source/drain region, respectively; \( C_{ox} \) is the oxide capacitance per unit area; \( Y \) is the effective thickness of inversion and accumulation carriers; \( N_D \) is the dopant concentration in the source/drain region; \( V_{FBn} \) is the flat-band voltage in the source/drain region. The \( S_{\text{max}} \) can be approximated by (referred to (3))

\[
S_{\text{max}} \approx k_3 (V_{GS} - V_T)^{-1}
\]

(17)

where \( k_3 \) is a constant, and we can evaluate \( S_{\text{jun}} \) from (17) simply by considering the channel resistance reduced by the built-in potential of the source/drain junction

\[
S_{\text{jun}} \approx k_3 (V_{GS} - V_T + V_{bip})^{-1}
\]

(18)

where \( V_{bip} \) is the built-in potential in the channel side. Substituting (15)-(18) into (14) and letting \( dA/dS_{\text{max}} = 0 \), after some manipulations we have

\[
(V_{GS} - V_T)^{-\frac{3}{2}} = \frac{1}{3} \left[ (V_{GS} - V_T)^{-\frac{3}{2}} + \left( \frac{qN_D Y}{C_{ox}} + V_{GS} - V_{FBn} \right)^{-\frac{3}{2}} \right]
\]

\[
\times (V_{GS} - V_T + V_{bip})^{-1}
\]

\[
+ \frac{2}{3} \left[ (V_{GS} - V_T)^{-\frac{3}{2}} + \left( \frac{qN_D Y}{C_{ox}} + V_{GS} - V_{FBn} \right)^{-\frac{3}{2}} \right]
\]

\[
\times (V_{GS} - V_T + V_{bip})^{-2}.
\]

(19)

Substituting \( Y \) [13], \( V_T \), \( V_{FBn} \) and \( V_{bip} \) into (19), we can solve \( V_{GS} \) by the iteration method. The results of the relationship among \( V_{GS} - V_T \), \( N_D \) and \( N_A \) (dopant concentration in the channel region) are shown in Fig. 7. The adequate gate overdrive to determine \( \Delta L_{\text{met}} \) for a fixed surface channel doping increases with the source/drain doping, because a larger gate overdrive is needed to accumulate the carrier density comparable to source/drain dopant concentration for heavily doped source/drain region, as shown in Fig. 4, where the higher source/drain doping results in weaker modulation for gate overdrive on the source/drain region. On the other hand, the gate modulation in the channel region becomes difficult as the gate overdrive increases due to strong inversion. So, a larger gate overdrive for heavily doped source/drain is needed to have \( dA/dS_{\text{max}} \) approaching to zero for extracting \( \Delta L_{\text{met}} \). This also can be observed from (13), in which \( R_{c1} + R_{c2} \) can be approximated by \( W_p(S_{\text{max}} - S_{\text{jun}}) \), as shown in Fig. 5, where \( W_p \) in (15) and \( S_{\text{max}} \) in (17) are independent of source/drain doping. Although \( S_{\text{jun}} \) in (18) depends on source/drain doping through \( W_n \) in (16), and this indicates that the gate modulation becomes weak when source/drain doping increases. In this situation, a weak gate modulation for \( R_{c1} + R_{c2} \) is needed to compensate it to let \( dA/dS_{\text{max}} = 0 \), which requires a higher gate overdrive.
On the other hand, the lower source/drain doping requires a lower gate overdrive to determine $L_{\text{met}}$.

For the channel concentration varies as large as two orders in magnitude, however, the adequate gate overdrive to determine $\Delta L_{\text{met}}$ does not show a large variation. This is convenient for our extraction algorithm, and we can determine $\Delta L_{\text{met}}$ without taking care of the channel doping. Moreover, the $n^-$ region doping for LDD devices is around $10^{18}$ cm$^{-3}$, and the adequate gate overdrive is about 1.5 V. For conventional devices, the gate overdrive must be large enough to about 5 V. Therefore, the principles for determining $\Delta L_{\text{met}}$ from $\Delta S_{\text{eff}}$ are verified again. Simulation results from Fig. 4 and other cases are also marked in Fig. 7, the results agree well with those using the analytic model evaluation. Therefore, the deduced range of gate overdrive is a useful reference for our extraction algorithm.

In general, the parasitic source/drain resistance extracted from the algorithm described in the previous section will be smaller than the exact value (if $\Delta L_{\text{met}}$ is correct). This can be observed from (10), if we let $L_M = \Delta L_{\text{met}}$, $R_T$ will be equal to $2R_{\text{es}}+2R_n-R_{\text{es}1}-R_{\text{es}2}$ and this value is smaller than $R_P = 2R_{\text{es}}+2R_n$ by $R_{\text{es}1}+R_{\text{es}2}$. So, we can predict that the extracted $R_P$ will deviate from its exact value, especially when the gate overdrive is small and the deviation is extremely large (Fig. 9). However, the extracted $R_P$ is very accurate at high gate overdrive.

IV. EXTRACTION RESULTS

The parameters given in our simulation are listed in Table I for conventional and LDD MOSFET's, and the definitions for the parameters are given in [11]. The mask channel lengths used are $L_M = 1.5, 1.2, 1.0, 0.8, 0.6 \mu$m. The extraction results for conventional and LDD MOSFET's with and without $V_T$ correction are all shown in Fig. 8. The $\Delta L_{\text{eff}}$ for conventional devices approaches to $\Delta L_{\text{met}}$ at around $V_{GS} - V_T = 5$ V, this agrees with the conclusions in the previous analysis (Fig. 7). The $V_T$ correction is not important because $R_P$ of conventional device is small. For LDD devices without $V_T$ correction, $\Delta L_{\text{eff}}$ is always smaller than $\Delta L_{\text{met}}$. After $V_T$ correction, $\Delta L_{\text{eff}}$ is equal to $\Delta L_{\text{met}}$ at a gate overdrive of about 1 V. The gate overdrive does not precisely agree with the analysis (Fig. 7) due to the assumptions of constant $R_P$ and $\mu$, and the error is introduced in the extraction process. For convenience without losing the precision of $\Delta L_{\text{met}}$ extraction, the maximum of $\Delta L_{\text{eff}}$ is chosen to be $\Delta L_{\text{met}}$ for LDD MOSFET's. On the contrary, we regard $\Delta L_{\text{eff}}$ at high gate overdrive (e.g., 5 V) as $\Delta L_{\text{met}}$ for conventional devices. However, it is not adequate to choose a very high gate overdrive because $S_{\text{max}}$ (averaged channel resistance) decreases very slowly at high gate overdrive, therefore $d\Delta S/dS_{\text{max}}$ is prone to induce enormous error by noise. On the other hand, as shown in Fig. 4(b), $d(R_{\text{es}1}+R_{\text{es}2})/dS_{\text{max}}$ approaches to zero at high gate overdrive, but $2dR_n/dS_{\text{max}}$ increases slowly. If a very high gate overdrive is chosen, $\Delta L_{\text{met}}$ will be underestimated. This means that at the very high gate overdrive a part of source/drain region becomes channel region, therefore reducing $\Delta L_{\text{eff}}$. In practice, we take the average of $\Delta L_{\text{eff}}$ in the range of 4~5 V in order to reduce the noise and the possible error.

### Table I

<table>
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<th>Parameter</th>
<th>Value</th>
<th>Parameter</th>
<th>Value</th>
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</tr>
<tr>
<td>$R_{\text{DS}}$ (10$^8$ cm$^{-3}$)</td>
<td>5.220</td>
<td>$R_{\text{DS}}$ (10$^{-4}$ cm)</td>
<td>10</td>
</tr>
<tr>
<td>$R_{\text{es}}$ (10$^{-4}$ cm$^{-2}$)</td>
<td>2.171</td>
<td>$\Delta L_{\text{met}}$ (\mu$m$)</td>
<td>0.2</td>
</tr>
<tr>
<td>$t_{\text{ox}}$ (10$^9$ cm$^{-2}$)</td>
<td>1.669</td>
<td>$\Delta L_{\text{met}}$ (\mu$m$)</td>
<td>0.64</td>
</tr>
<tr>
<td>$R_{\text{es}}$ (10$^8$ cm$^{-3}$)</td>
<td>1.169</td>
<td>$R_{\text{DS}}$ (10$^{-4}$ cm)</td>
<td>0.152</td>
</tr>
<tr>
<td>$R_{\text{es}}$ (10$^{-4}$ cm$^{-2}$)</td>
<td>3.027</td>
<td>$R_{\text{DS}}$ (10$^{-4}$ cm)</td>
<td>0.221</td>
</tr>
</tbody>
</table>

*For LDD devices*
Fig. 9. Comparisons between the computed and extracted parasitic resistance versus gate overdrive for conventional and LDD MOSFET's.

The extracted and computed (from simulator) $R_P$ are plotted in Fig. 9. As indicated, the larger $R_P$ values emphasize the importance of $V_T$ correction for LDD devices. For conventional devices, $R_P$ at low gate overdrive is smaller than that at high gate overdrive. This is due to large $R_{c1}$, $R_{c2}$ and small $R_n$ at low gate overdrive. However, for LDD devices, the behaviors of $R_{c1}$ and $R_{c2}$ are similar to those of conventional devices, but $R_n$ is large enough to compensate $R_{c1}$ and $R_{c2}$. So $R_P$ still increases; unlike the conventional devices, it decreases as the gate bias is reduced. Anyway, the extracted $R_P$ is always smaller than the computed results using a simulator at any gate overdrive for both devices, because we cannot evaluate $R_{c1}$ and $R_{c2}$.

To verify the validity of this extraction algorithm for various device structures, many cases are simulated by the SUMMOS. The conventional devices consisting of different oxide thicknesses and channel concentrations are fabricated, and the I-V characteristics are measured by HP-4145B. Applying our extraction algorithm to the I-V characteristics of these devices, the extraction results are listed in Table III. In Table III, wafer Nos. 5, 17 and 32 have different oxide thicknesses with the same channel doping, the extraction results show that $\Delta L_{met}$ is 0.170 $\mu$m with small variation. A quite reasonable conclusion can be drawn for these cases—the oxide thickness doesn’t influence $\Delta L_{met}$. However, wafer Nos. 15, 17 and 19 have different channel implantation doses with the same oxide thickness, the extracted $\Delta L_{met}$ value varies from 0.170 to 0.195 $\mu$m. In theory, the higher channel concentration should reduce $\Delta L_{met}$ slightly. This phenomenon is not shown in Table III. The discrepancy may be resulted from the nonuniform channel profile in the lateral direction due to the reverse short channel effect, which is more serious for heavy channel implantation [14].

The test devices with the LDD structure are also fabricated and examined, as shown in Table III, in which a novel channel-length extraction method using the charge pumping technique [15] is also performed. Comparing with our extraction results, it is shown that very good agreements are obtained.

V. CONCLUSION

A new extraction algorithm for the metallurgical channel length and the parasitic resistance of conventional and LDD MOSFET's is described. With our proposed technique, the errors induced by channel-length uncertainty and the effects of parasitic source/drain resistance on the threshold voltage are reduced. A 2-D numerical analysis is performed to analyze the factors affecting the effective channel length, and the ex-
traction principles for $\Delta I_{\text{net}}$ are proposed. The principles for
extracting the metallurgical channel length deduced from the
2-D numerical analysis are also evaluated by a simple analytic
model. Comparing with 2-D numerical analysis, the analytic
model evaluation is proven to be a reasonable approximation.

The proposed extraction algorithm has been verified by
the simulated I-V characteristics, and the error is within 0.01
$\mu$m. Moreover, the parasitic source/drain resistance is also
extracted, and it is shown that smaller parasitic resistance at
low gate overdrive is inevitable. Compared with the computa-
tion results, the extraction results are fairly accurate. Applying
this extraction algorithm to the experimental devices and
comparing with the results extracted by the charge pumping
method, it is shown that very good agreements between these
two methods are obtained.

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