O₂-Plasma Passivation Effects on Polysilicon Thin Film Transistors Using Ion Plating Method

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ABSTRACT

A novel method has been developed for efficiently reducing defect density in polysilicon thin film transistors using ion plated oxides as capping layers. The characteristics of these novel thin film transistors are superior to those of thin film transistors with plasma-enhanced chemical vapor deposited tetraethylorthosilicate capping oxides due to an in situ O₂-plasma passivation effect during ion plating oxide deposition. The passivation effect of a NH₃ plasma on the novel devices was also studied. The in situ ion plating O₂ plasma shows a better passivation efficiency on trap states than the NH₃ plasma. Polysilicon thin film transistors with ion plating capping oxides are hardly degraded even when stressed with a bias of 20 V at 100°C.

Introduction

It is well known that polycrystalline silicon (poly-Si) films have a high concentration of grain boundary defects as well as intragrain defects. As a result of the high density of trapping states in poly-Si films, it has been found necessary to passivate them to improve poly-Si thin film transistor (TFT) performance. Various technologies have been proposed to reduce trapping states in poly-Si films, such as hydrogenation, O₂ plasma, and NH₃ plasma. So far, the most popular passivation procedure has been to expose devices to hydrogen plasma. However, it takes a long time to achieve satisfactory performance, and the improvement shows a tendency to saturate. In addition, hydrogenated TFTs are quite prone to reliability problems due to carrier-induced trap states in poly-Si channels. These shortcomings greatly limit the practical application of H₂-plasma passivation. In recent years, the passivation effect of an O₂ plasma has attracted much attention because of its better passivation efficiency and stability. It has been suggested that O₂-plasma treatment can improve the performance of poly-Si TFTs by passivating deep states and tail states. Furthermore, it has been reported that after an O₂-plasma treatment, subsequent treatment with a H₂ plasma was even more efficient in passivating trap states in poly-Si films.

Recently, a low-temperature ion plating (IP) method has been proposed to prepare high-performance oxide films. IP oxide has been shown to be feasible for application as a poly-Si TFT gate insulator, and to contribute to excellent device characteristics. Since an O₂ plasma is present in the chamber during IP oxide deposition, it can be expected to have the effect of trap-state passivation on the poly-Si layer. In this paper, we try to apply IP oxides as capping layers on poly-Si TFTs, and investigate passivation effects owing to the in situ O₂ plasma. The passivation of dangling bonds is examined by electron spin resonance (ESR) measurement. NH₃-plasma passivation effects and the reliability of the novel poly-Si TFTs are also studied.

Experimental

Preparation of IP oxide.—IP oxide films were prepared using the ion-plating system (Balzers BAP 800). Since an O₂ plasma is present in the chamber during IP oxide deposition, it can be expected to have the effect of trap-state passivation on the poly-Si layer. In this paper, we try to apply IP oxides as capping layers on poly-Si TFTs, and investigate passivation effects owing to the in situ O₂ plasma. The passivation of dangling bonds is examined by electron spin resonance (ESR) measurement. NH₃-plasma passivation effects and the reliability of the novel poly-Si TFTs are also studied.

![Fig. 1. Schematic diagram of the ion-plating system (Balzers BAP 800).](image)
Fabrication of poly-Si TFTs.—Conventional co-planar N-channel poly-Si TFTs were prepared using the following procedures. The cross-sectional structure of the poly-Si TFTs is shown in Fig. 2. A 100 nm thick low-pressure chemical vapor deposition (LPCVD) amorphous Si layer was deposited on thermal oxide at 550°C using SiH₄ gas. Recrystallization was performed at 600°C for 24 h using the solid-phase crystallization (SPC) method. A 40 nm thick liquid-liquid phase deposited (LPD) oxide layer was grown on the island-patterned SPC layer at 18°C, and then densified at 600°C for 1 h in O₂ ambient. A 300 nm thick poly-Si layer was deposited using the LPCVD method at 620°C after the poly-Si gates were patterned, the source/drain and gate regions were implanted with phosphorus ions (40 keV, 5 × 10¹⁵ cm⁻²) by self-aligned technology. Dopant activation was performed at 600°C for 24 h in N₂ ambient. The 500 nm thick capping layer was deposited at a rate of 0.2 nm/s for about 42 mm using the IP method. The temperature of the substrate was 23°C at the beginning of the IP oxide deposition process, and increased to 110°C at its end. After contact holes were opened, aluminum electrodes were prepared and sintered at 400°C for 30 min in N₂ ambient. The maximum processing temperature was 620°C.

For comparison, poly-Si TFTs with 32.5 nm thick LPD gate oxides and 500 nm thick tetraethyl orthosilicate (TEOS) capping oxides were prepared. The TEOS oxide was deposited at 300°C using the plasma-enhanced CVD (PECVD) method. Hydrogenation by the NH₃-plasma treatment was performed in a parallel-plate reactor at 40°C and the refractive index were measured by ellipsometer, while the chemical structure was analyzed by Fourier transform infrared spectrophotometer (FTIR). The etching rate was examined with P-etch solution (48% HF: 70% HNO₃: H₂O = 3:2:60) at room temperature. To investigate the electrical characteristics of these oxides, metal-oxide-silicon (MOS) capacitors with aluminum gates were prepared. The current-voltage characteristics were measured with an HP4145B and a Keithley Package 82 system, respectively. The IP oxides were used as capping layers in poly-Si TFTs.

Results and Discussion

| Table I. Physicochemical and electrical properties of IP and thermal oxides. |
|-----------------|----------------------|----------------------|
| Ion plating oxide | Thermal oxide |
| FTIR stretching frequency (cm⁻¹) | 1056 | 1076 |
| Refractive index | 1.463 | 1.463 |
| P-etch rate (Å/s) | 4.9 | 2.0 |
| Leakage current density, at 4 MV/cm (Å/cm²) | 8.5 × 10⁻⁹ | 1.1 × 10⁻⁹ |
| Dielectric breakdown field (MV/cm) | 9.3 | 9.4 |
| Dielectric constant at 1 MHz | 4.5 | 3.9 |
| Flatband voltage (V) | -0.87 | -1.68 |
| Interface state density (eV⁻¹ cm⁻²) | 1.85 × 10¹⁰ | 4.50 × 10¹⁰ |

Characteristics of poly-Si TFTs with IP oxides as capping layers.—Figure 3 shows the transfer characteristics of both poly-Si TFTs (W/L = 20/5 μm) with IP and with TEOS oxides as capping layers, respectively. The characteristic of IP oxide is feasible for application as a capping layer in poly-Si TFTs.

ESR measurements.—The dangling bond density in poly-Si films was measured by room-temperature ESR absorption spectra (X-band) before and after the in situ O₃-plasma treatment. Poly-Si films were prepared by the LPCVD method at 620°C to a thickness of 300 nm onto thermally oxidized Si-wafer. IP oxide was directly deposited on the poly-Si films, and then annealed at 400°C for 30 min in N₂ ambient. This is because devices were sintered after metallization in TFT fabrication processes. The deposition condition of IP oxide was the same as that of the IP capping oxide for poly-Si TFTs. Before ESR measurements, the IP oxide and the back side poly-Si/thermal oxide were removed.

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**Fig. 2. Cross-sectional structure of the poly-Si TFTs.**

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**Fig. 3. Typical transfer characteristics (I_d, V_g) at V_d = 15 V for poly-Si TFTs (W/L = 20/5 μm) with IP and with TEOS oxides as capping layers without hydrogenation.**

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poly-Si TFTs (W/L = 20/5 μm) with IP and with TEOS capping layers before and after 8 h NH₃-plasma treatment.

<table>
<thead>
<tr>
<th>Capping layer</th>
<th>NH₃ plasma treatment</th>
<th>V_DS (V)</th>
<th>S.S. (V/dec)</th>
<th>I_DS/I_OFF</th>
<th>μ handjob (cm²/V s)</th>
<th>N₁ (cm⁻³)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP</td>
<td>No</td>
<td>4.23</td>
<td>0.94</td>
<td>4.10 × 10⁴</td>
<td>24.3</td>
<td>1.05 × 10¹²</td>
</tr>
<tr>
<td></td>
<td>8 h</td>
<td>2.33</td>
<td>0.77</td>
<td>3.18 × 10⁵</td>
<td>25.6</td>
<td>8.37 × 10¹²</td>
</tr>
<tr>
<td>TEOS</td>
<td>No</td>
<td>11.0</td>
<td>1.61</td>
<td>2.09 × 10⁶</td>
<td>9.71</td>
<td>2.70 × 10¹³</td>
</tr>
<tr>
<td></td>
<td>8 h</td>
<td>5.49</td>
<td>0.84</td>
<td>4.75 × 10⁶</td>
<td>14.4</td>
<td>1.05 × 10¹³</td>
</tr>
</tbody>
</table>

Figure 5 shows transconductance (Gm) as a function of gate bias at V_DS = 0.1 V for both IP capped and TEOS capped poly-Si TFTs (W/L = 20/5 μm). The maximum Gm is 7.6 × 10⁻⁴ A/V for the IP capped device, while it is 3.8 × 10⁻⁴ A/V for the TEOS capped device. In addition, the gate voltage yielding the maximum Gm is also comparatively small for the IP capped device.

Figure 6 shows the output characteristics (I_DS-V_DS) with V_GS-V_DS = 2 V and 6 V for both IP capped and TEOS capped devices (W/L = 20/10 μm). In the curves of IP capped device, both the high slope in the linear region and the high saturation current imply that channel conductance is high. Generally in poly-Si TFTs, the transport of free carriers between the grains is impeded by the potential barrier owing to the trap states at the grain boundaries. The lower barrier height makes On-state performance respond much faster to the applied gate and drain biases. In the IP capped device, the increases in transconductance and channel conductance can be attributed to the lowering of barrier height due to the reduction of trap-state density.

Figure 7 shows the transfer characteristics in the low gate bias region at V_DS = 5, 10, and 15 V for both IP capped
and TEOS capped poly-Si TFTs without hydrogenation (W/L = 20/5 μm). In the case of V_d = 5 V, the IP capped device shows a rather flat leakage characteristic independent of gate bias except for a higher minimum leakage current (I_min). The minimum leakage current is dominated by the channel resistance. In this region, the barrier height that transfer carriers have to surmount at the grain boundary will govern the magnitude of the minimum leakage current. The higher the barrier height, the lower the leakage current observed. Because there is a lower trap-state density in the IP capped device, the barrier height and thus the channel resistance are lower than those in the TEOS capped device. Thus, I_min is a little higher in the IP capped device. When the drain voltage was increased to 15 V, I_min was dominated by Frenkel-Poole emission in the drain junction depletion region. Frenkel-Poole emission current is contributed by field-enhanced thermal excitation of trapped holes in the valence band. Owing to the lower trap-state density, the IP capped device exhibited a lower leakage current than the TEOS capped device at V_d = 15 V. In addition, when the drain bias was increased, the leakage current in the IP capped device also showed a smaller variation due to its lower trap-state density.

Some authors have reported that for poly-Si TFTs an O2-plasma-treatment cannot passivate grain boundary defects according to the unchanged ESR signals of defect density. The O2-plasma can only oxidize the device surface and grow a thin SiO2 layer, which can reduce the surface leakage current. However, our studies show that the improvement in IP capped TFTs is assuredly due to the in situ O2-plasma passivation effect. As shown in Fig. 4, the reduced spin density owing to capping IP oxide indicates that the IP process possesses passivation effects. In addition, to clarify the influence of IP process and surface cleaning, we also prepared a IP/TEOS capped TFT sample. After capping IP oxide on TFTs and annealing at 400°C for 30 min in N2 ambient, we removed the IP oxide using HF solution and then deposited TEOS capping oxide. For the TEOS capped TFT, we also ever removed the native oxide on the surface before capping TEOS oxide. It means that the IP/TEOS capped TFT and the TEOS capped TFT have the same surface plasma and device surface and grow a thin SiO2 layer, which can reduce the surface leakage current. However, our studies show that the improvement in IP capped devices is more apparent after the NH3-plasma treatment. The key characteristic parameters after the NH3-plasma treatment are also summarized in Table II. Although the improvement in the TEOS capped devices is more apparent after the NH3-plasma treatment, in total the characteristics of IP capped devices are still superior to those of TEOS capped devices. For both IP capped and TEOS capped TFTs, the minimum leakage current did not well decrease after 8 h NH3-plasma treatment. It can be attributed to the insufficient passivation time. Generally, I_min is dominated by the total resistance in active layer. The total resistance is composed of the junction resistance at the drain junction and the channel resistance. The lower the channel resistance, and then the higher I_min is observed. However, after NH3-plasma passivation the leakage junction depletion can also be passivated resulting in an increased junction resistance. When the passivation is insufficient, I_min is dominated by the channel resistance. The decrease of trap states after NH3-plasma treatment can result in the reduction in barrier height. The lower the barrier height, the lower the channel resistance, and then the higher I_min is observed. However, after NH3-plasma passivation the leakage junction depletion can also be passivated resulting in an increased junction resistance. When the passivation is insufficient, I_min is dominated by the channel resistance and become reduced.

Figure 9 shows a comparison of subthreshold swing between IP capped and TEOS capped devices as a function of NH3-plasma passivation time. It was found that the improvement in the IP capped device saturated after 2 h.
However, there was a dramatic improvement in subthreshold swing for the TEOS capped device when the NH$_3$-plasma passivation time was increased. The threshold voltage change tendencies for both types of device after the NH$_3$-plasma treatment were similar to those for subthreshold swing. The apparent improvement in S.S. and $V_{th}$ for TEOS capped devices can be attributed to a reduction of midgap deep states after NH$_3$-plasma passivation. The improvement for IP capped devices appears smaller and quickly saturated because many deep states were passivated by the in situ O$_3$ plasma during IP capping oxide deposition, and only some residual deep states could be further passivated by the NH$_3$-plasma treatment. Figure 10 shows the changes in field-effect mobility as a function of NH$_3$-plasma passivation time for IP capped and TEOS capped devices. The gradual increase in $\mu_{FE}$ for the TEOS capped devices indicates that some tail states were passivated by the NH$_3$-plasma treatment. However, the improvement saturated after the 8 h NH$_3$-plasma treatment, and the saturated $\mu_{FE}$ was still smaller than that of the as-fabricated IP capped device. This indicates that the in situ O$_3$-plasma treatment can more effectively passivate the tail states in the poly-Si films than the NH$_3$-plasma treatment. Hence, the subsequent NH$_3$-plasma treatment nearly has no influence on $\mu_{FE}$ for IP capped devices. The above results support the feasibility of fabricating excellent poly-Si TFTs without additional hydrogenation.

For PECVD TEOS capped TFTs, it must be clarified whether the requirement of more hydrogen passivation is due to PECVD TEOS charge damage. If there is serious charge damage during PECVD TEOS process, the characteristics of IP/TEOS capped TFTs will be worse than those of IP capped TFTs. However, we did not find this phenomenon. Therefore, the PECVD TEOS charge damage can be ignored.

Stability of in situ O$_3$ plasma passivation. The stability of poly-Si TFTs is of significant importance from a long-term operation standpoint. It has been reported that H$_2$ plasma treated devices exhibited higher degradation rates than O$_3$-plasma treated devices. In this section, the stability of as-fabricated IP capped TFTs and NH$_3$-plasma treated TEOS capped TFTs is investigated.

To accelerate degradation and investigate thermal stability, both the as-fabricated IP capped devices and the 10 h NH$_3$-plasma treated TEOS capped devices were stressed with $V_{ds} = V_{dd} = 20$ V at 150°C. Figure 11(a) and (b) show the changes in transfer characteristics for the two devices before and after stressing for $10^4$ s. The degradation of the TEOS capped devices is very noticeable. The S.S. increased from 0.82 to 1.27 V/dec, while the $V_{th}$ increased from 5.30 to 8.87 V because high-temperature dc stressing appears to break the Si-H bonds, resulting in additional trap states generated at grain boundaries. Hence, the stressing degrades the S.S. and $V_{th}$ characteristics of the TEOS capped devices toward prehydrogenated values. On the other hand, the degradation of the as-fabricated IP capped devices was slight because of the higher bond strength of Si-O bonds over that of Si-H bonds. Hence, fewer additional trap states were generated during high-temperature dc stressing for devices treated with in situ O$_3$-plasma passivation. Figure 12 shows the subthreshold swing degradation rate ($\Delta S.S.$) as a function of stress temperature for the as-fabricated IP and the NH$_3$-plasma treated TEOS capped devices under stressing at $V_{ds} = V_{dd} = 20$ V for $10^4$ s. $\Delta S.S.$ for the NH$_3$-plasma treated TEOS capped device appears very sensitive to and seriously affected by the stressing temperature. However, $\Delta S.S.$ for the IP capped device appears rather stable until the temperature exceeded 100°C. From this result, it can be concluded that the novel poly-Si TFTs with IP capping oxides indeed exhibit good stability even when stressed at high temperatures and high biases.

Conclusions

Poly-Si TFTs with IP oxides as capping layers exhibit excellent performance, which is due to in situ O$_3$-plasma passivation effect during IP process, not the material of IP oxide itself. The in situ O$_3$-plasma treatment effectively reduces the trap states in poly-Si films, resulting in a threshold voltage of 4.23 V, a subthreshold swing of 0.94 V/dec, a field-effect mobility of 24.3 cm$^2$/V s, and an On/Off current ratio of 4.10 $\times$ 10$^4$ without hydrogenation. Poly-Si TFTs with IP capping oxides also show a small increase in leakage current as drain bias is increased. Because most of the trap states (particularly the tail trap states) are passivated by the O$_3$ plasma, the improvement provided by the NH$_3$-plasma treatment of poly-Si TFTs with IP capping oxides is not very evident. It is feasible to fabricate these novel poly-Si TFTs without additional hydrogenation. The novel devices also show superior stability even under stressing at 100°C with high $V_{ds}$ and $V_{dd}$.

Acknowledgment

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Fig. 11. Changes in transfer characteristics ($I_D$-$V_G$) under stress of $V_{gs} = V_{ds} = 20$ V for $10^4$ s at $150^\circ$C for (a) TEOS capped devices after NH$_3$-plasma treatment and as-fabricated devices (W/L = 10/5 μm).

Fig. 12. Subthreshold swing degradation rates ($\Delta S.S.$, %) under stresses of $V_{gs} = V_{ds} = 20$ V for $10^4$ s at 25, 100, and 150°C for TEOS capped devices after NH$_3$-plasma treatment and as-fabricated IP capped devices (W/L = 10/5 μm).

REFERENCES


34. R. L. David, CRC Handbook of Chemistry and Physics:
Boron Diffusion in Compressively Stressed Float Zone-Silicon Induced by Si$_3$N$_4$ Films

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ABSTRACT

The effect of stress during annealing induced by Si$_3$N$_4$ films on boron diffusion in float zone-silicon has been studied and a correlation between vacancy concentration and compressive strain in the substrate has been clarified. From the results of Si$_3$N$_4$ film thickness and annealing temperature dependence on both boron diffusivity and stress in the substrates, boron diffusion was found to be retarded and the substrate was found to have high stress, having elastic compressive strain during annealing under Si$_3$N$_4$ films. These results indicate that excess vacancies are generated by elastic compressive strain, causing the retardation of interstitial-mediated diffusion of boron.

Introduction

Silicon nitride (Si$_3$N$_4$) films have been used as an oxidation mask and passivation materials in ultra-large-scale integration (ULSI) process technology. Si$_3$N$_4$ films deposited on Si have high stress and produce effects on Si substrates such as the generation of dislocations$^1$ during thermal annealing.

With the shrinkage of device dimensions, precise control of dopant profiles in the substrate becomes more and more important. Therefore, it is very important to study the effects of stress in the films on both the Si substrate surface and on dopant diffusion.

It is known that chemical vapor deposition (CVD) silicon nitride films develop intrinsic stress during deposition and thermal stress during annealing, influencing dopant diffusion. Ahn et al.$^2$ reported retarded diffusion of P, enhanced diffusion of Sb, and an increase in the shrinkage rate of extrinsic stacking faults in float zone (FZ)-Si under the low-pressure CVD (LPCVD) SiN$_x$ films by varying the stress level in the films with different values of x. Osada et al.$^3$ investigated retarded diffusion of boron in FZ-Si under electron cyclotron resonance (ECR) plasma CVD Si$_3$N$_4$ films by changing annealing temperature, annealing time, and the film thickness in detail.

These reports suggest that stress of Si$_3$N$_4$ films disturbs the point defect concentration in the silicon substrate during annealing. However, stress of Si$_3$N$_4$ films was measured only after the film deposition. The change of the intrinsic stress of the films and the actual stress during annealing have not been taken into consideration.

In this study, we first investigated the stress of Si$_3$N$_4$ films deposited by ECR plasma CVD on FZ-Si as a function of the film thickness and the thermal history. Then, the effect of stress induced by Si$_3$N$_4$ films on boron diffusion in FZ-Si was studied by changing Si$_3$N$_4$ film thickness and annealing temperature. Correlation between the stress at the surface of the Si substrate and the retardation of boron diffusion has been clarified from these results. Retarded diffusion of boron will be discussed in terms of the excess vacancy generation.

Experimental

Substrates used were p-type, 525 $\mu$m thick (100) FZ-Si with resistivity of 4 $\sim$ 6 $\Omega$ cm for the measurement of boron diffusion and the observation of defects at the surface of the substrates. SiO$_2$ films with thickness of 50 nm were grown in dry O$_2$ at 1000°C for 60 min on samples. Boron ions were implanted into samples through SiO$_2$ with a dose of $3 \times 10^{15}$/cm$^2$ at 20 keV. This dose affirmed the so-called intrinsic conditions, in which the carrier concentration is smaller than the intrinsic carrier concentration at annealing temperatures. Samples were annealed in N$_2$ at 900°C for 30 min to remove the ion implantation induced damage. After removing SiO$_2$ films at the back side and at the top side selectively, Si$_3$N$_4$ films were deposited on samples at the top side by ECR plasma CVD at 100°C using SiH$_4$ and N$_2$. ECR plasma CVD allows the deposition of thin films at lower temperature at low gas pressures in the range of $10^{-2}$ to $10^{-3}$ Torr, and does not need any thermal reaction.$^1$ Using this CVD system, high quality Si$_3$N$_4$ films can be obtained. The thickness of Si$_3$N$_4$ films was set to be 50, 100, 160, 430, and 790 nm. The structure of samples is shown in Fig. 1. The areas masked with SiO$_2$-Si$_3$N$_4$ films and masked with Si$_3$N$_4$ films were defined as the ON-area and the N-area, respectively.

Substrates used for the measurement of displacement were p-type, 625 $\mu$m thick (100) FZ-Si with resistivity of 11 to 25 $\Omega$ cm. They were mirror-polished at both sides and cut into a strip with length of 8 cm and width of 1 cm. Si$_3$N$_4$ films were deposited on the Si substrate by ECR plasma CVD with the same conditions mentioned above. The structure of samples is shown in Fig. 1.

Thermal annealing was performed for all samples in N$_2$ at temperatures ranging from 900 to 1100°C for 360 min. Boron profiles were measured by secondary ion mass spectroscopy (SIMS) at 6500. Stressed-induced...