is close to about 1.2 (\(\Delta r_1/\Delta r_2\)), the best CP operation can be obtained. Axial ratio is 0.68 dB at 2540 MHz centered. The measured axial ratio and gain for the proposed antenna are shown in Figure 3 and the design dimensions and CP performance are also summarized in Table 1.

4. CONCLUSION

A design of circularly polarized microstrip antenna with asymmetric ring-sector two-pair slots embedded on the ground plane for increasing antenna gain is presented. The embedded ring-sector slots on the ground plane can increase the radiation efficiency by decreasing quality factor of proposed antenna. Also, the CP performance can be easily adjusted by selecting proper slot length ratio of the asymmetric ring-sector slots. The measured peak gains of the proposed antenna and the reference antenna are 5.0 and 2.2 dBi, respectively. The radiation patterns of proposed antenna measured at 2540 MHz are plotted in Figure 4 and the broadside radiation patterns with good axial ratio are found at the two orthogonal planes.

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CALIBRATION 90 nm NODE RF MOSFETS, INCLUDING STRESS DEGRADATION

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Received 26 July 2006

ABSTRACT: Using a microstrip line layout, a low minimum noise figure \((NF_{\text{min}})\) of 0.51 dB, at 10 GHz, was directly measured for 90 nm node NMOSFETs (65 nm physical gate length). The \(NF_{\text{min}}\) was located at the peak \(f_p\) of 152 GHz, coinciding with the peak transconductance \((g_m)\). On the basis of these measurements, a self-consistent model of the DC \(I-V, S\)-parameters, and \(NF_{\text{min}}\) was developed, including the changes after hot-carrier stress. © 2007 Wiley Periodicals, Inc. Microwave Opt Technol Lett 49: 604–607, 2007; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.22209

Key words: \(NF_{\text{min}}; f_p; MOSFETS; stress; model\)

1. INTRODUCTION

As silicon technology has evolved, the device performance has improved to the point where Si RF MOSFETs [1–8] are now widely used in wireless communication ICs. RF transistors, when compared with their digital and low frequency analog counterparts, require more accurate device models and supporting measurements. This arises from the tight specifications for impedance matching, low noise, and high gain. In addition, the modeling of the RF performance degradation of transistors under continuous operation is vital for RF IC design [8–10]. Here, we have modeled multiple-gate-fingered [5, 6] 90 nm node MOSFETs to obtain self-consistent DC, RF, and \(NF_{\text{min}}\) parameters, close to the measured data. To obtain accurate as-measured \(NF_{\text{min}}\), a microstrip transmission line layout [7, 8] was used to shield the RF noise generated in the lossy Si substrate [5, 6]. We obtained \(NF_{\text{min}}\) of 0.51 dB at 10 GHz for 90 nm node RF MOSFETs (65 nm physical gate length) without any de-embedding. This is one of the lowest reported \(NF_{\text{min}}\) in CMOS [1–3], and it is due to the successful shielding of the noise arising from the low resistivity Si substrate. The degradation caused by hot-carrier-induced stress was determined after 5000 s at \(V_{gs} = 1.4\) V and \(V_{ds} = 2.1\) V, and gave a 10% drive current reduction [8–10]. We obtained a good match between the measured and modeled DC \(I-V, S\)-parameters, and \(NF_{\text{min}}\), once the current degradation was included. Our self-consistent model can be used in circuit design as a tool for predicting the performance before and during continuous operation.

2. EXPERIMENTAL PROCEDURES

The multiple-fingered 90 nm node CMOS technology used in this study has a 65 nm physical gate length. We used the multiple 16-gate-finger layout to reduce the gate-resistance-generated thermal noise [5, 6]. To screen out the dominant thermal noise (from the parasitic substrate resistance) of the RF probing pads and the CPW line, the 65 nm devices were designed in a microstrip line layout [7, 8] instead of conventional CPW layout [5, 6]. In this way accurate intrinsic MOSFET \(NF_{\text{min}}\) measurements can be obtained directly [8]. This also permits an accurate determination of the degradation of \(NF_{\text{min}}\) following electrical stress. The device char-
Characteristics were measured by using an HP 4155C for DC I-V, an HP 8510C network analyzer for S-parameters and ATN-NP5B for noise parameter measurements [5–8]. The devices were stressed electrically at $V_{ds} = 2.1$ V and $V_{gs} = 1.4$ V for 5000 s, and then re-measured. A self-consistent DC to RF model was developed, which had a BSIM core and had parasitic RC elements to the gate, drain, and body to simulate the device characteristics before and after stress.

3. RESULTS AND DISCUSSION

Figure 1 shows the $I_d$ – $V_d$ characteristics for a 16-gate-finger 90 nm NMOSFET, before and after stress. A high drive current of 22.5 mA is observed because of the small gate length and multiple parallel gate fingers. After hot-carrier stress, the saturation drain current $I_{d,\text{sat}}$ decreased to 20.4 mA. The drain current decrease is due to interface state ($N_d$) and oxide trap generation at the drain side of the device.

Figure 2 illustrates the time dependence of the transconductance ($g_m = \partial I_d/\partial V_{gs}$) and saturation current ($I_{d,\text{sat}}$) for 90 nm node RF MOSFETs, under the hot-carrier stress conditions of $V_{ds} = 2.1$ V and $V_{gs} = 1.4$ V. The above stress conditions gave an accumulated $\Delta g_m$ of 14% and $\Delta I_{d,\text{sat}}$ of 10% after 5000 s. During the stress, both $g_m$ and $I_{d,\text{sat}}$ degrade monotonically with increasing stress time and the amount of degradation follows a power law. Such dependence is typical for hot-carrier stress that originates from interface charge generation, and the resulting decrease of the electron mobility. The modeled DC $I$-V characteristics, before and after stress, are also shown in Figure 1.

The effect of the hot-carrier stress is not only important for DC characteristics but it also has a large impact on the RF performance and impedance matching in circuits. The degraded performance (DC to RF) needs to be predicted by device modeling, particularly when the failure criteria is targeted in the range of 10–20% of $I_{d,\text{sat}}$.

Figure 3 depicts the measured and modeled S-parameters of 16-gate-fingered 90 nm RF MOSFETs before and after stress. We found that $S_{21}$ and $S_{22}$ displayed more significant changes than $S_{11}$ and $S_{12}$, after the hot-carrier stress. The effect of the stress on $S_{21}$...
as-measured NFmin was only 0.51 dB at 10 GHz. Figure 5(b) shows the NFmin at 10 GHz, 

\[ NF_{\text{min}} \approx 1 + 2y(1 + g_mR_f) \gamma f_T \] 

Again, close agreement between measured and modeled NFmin was obtained for the unstressed and stress devices, as is also shown in Figure 5.

4. CONCLUSION

We have measured and modeled the effects of hot-carrier stress on the DC to RF performance of 16-gate-fingered 90 nm node RF MOSFETs. Close agreement was obtained between the measured and modeled \( f_V, S \)-parameters, and NFmin data. This approach should be useful in predicting the RF performance degradation of MOSFETs in a circuit when operated under continuous bias.

ACKNOWLEDGMENT

We thank Chip Implemental Center and Dr. G. W. Huang at the National Nano-Device Laboratory for the help with the RF measurements.

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Sensitivities of charges and current densities for planar structures were obtained to solve the matrix equation, requiring \( O(N^3) \) computational load. Above techniques employ LU decomposition [5] to solve the matrix elements and its implementation into the optimization environment would require large amount of reprogramming of the current MoM simulation tools. To make the programming implementation easier, a feasible adjoint technique [3] combined with MoM was proposed in Ref. 4 to realize the full-wave sensitivity analysis. Above techniques employ LU decomposition [5] to solve the two matrix equations, requiring \( O(N^3) \) computation loads.

This article presents a full-wave technique to analyze sensitivities of multilayer planar structures. With the aid of iterative adjoint technique and the spatial Green’s functions in DCIM form [6, 7], the present technique has the following advantages: (1) the adjoint technique is employed to make the sensitivity analysis very easy to implement into the current MoM-based simulation tools; (2) the iterative scheme (generalized conjugate residual, GCR) is introduced to solve the matrix equation, requiring \( O(N^2) \) computation for each step. It would greatly save computation time if the iteration converges fast; (3) the spatial Green’s kernel in DCIM form makes it possible to investigate the performance sensitivity with respect to the geometrical parameters, which the Green’s function is dependent on. This case cannot be solved in Ref. 2. In the present study, sensitivities of \( S \)-parameters of a low-pass filter with respect to the design parameters are analyzed to validate the accuracy and efficiency of the present technique.

2. FORMULATION

MoM subject to the MPIE has been proved as an accurate and efficient technique to analyze properties of multilayer planar structures. Current density distribution on metal patch is first solved via linear matrix equation as

\[
\mathbf{Z}(x)\mathbf{I} = \mathbf{V}
\]  

where \( \mathbf{x} \) is a vector of design parameters, which need to be adjusted to optimize circuit performance. Elements in the impedance matrix \( \mathbf{Z} \) are obtained as

\[
Z_{ij} = j\omega e \int_{S_i} \int_{S_j} \mathbf{G}_i(r,r') \cdot \mathbf{f}(r') \cdot \mathbf{f}(r) ds'ds
+ \frac{1}{j\omega} \int_{S_i} \int_{S_j} \mathbf{G}_i(r,r') \cdot \mathbf{f}(r) \nabla \cdot \mathbf{f}(r) ds'ds
\]

where \( \mathbf{f}(r) \) and \( \mathbf{f}(r') \) are the RWG testing and basis functions, and \( S_i \) and \( S_j \) are their supports, respectively. \( \mathbf{G}_i \) and \( \mathbf{G}_j \) are the spatial Green’s functions in DCIM form for vector and scalar potentials respectively. Here, we use GCR iterative schemes to solve the matrix equation, which needs \( O(N^2) \) computation cost for each iterative step. The scattered field can be expressed as

\[
E_s = -j\omega \mathbf{A} - \nabla \Phi
\]

where the vector and scalar potentials can be obtained by using

\[
A(r) = \int_S \mathbf{G}_i(r,r') \cdot \mathbf{I}(r') ds'
\]

\[
\Phi = \int_S \mathbf{G}_i(r,r') \nabla \cdot \mathbf{I}(r') ds'
\]