CONTROL CIRCUIT OF SRAM AND OPERATING METHOD THEREOF

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ABSTRACT

A control circuit of SRAM and an operating method thereof are provided. The control circuit includes a memory array, a word-line driver, a boost circuit and a voltage level detecting circuit. The memory array includes a plurality of memory cells. Each memory cell includes a plurality of transistors. The word-line driver is to activate the word-line of the memory array for cell storage data access. The boost circuit is to provide the higher voltage source for the word-line driver and a first operating voltage for boosting the first operating voltage to a second operating voltage. The voltage level detecting circuit is detecting if the first operation voltage needed boosted with boost-operation and a detecting-trigger signal and controls the operating of the boost circuit based on the detecting-trigger signal, the first operating voltage and a predetermined voltage.
Figure 1

- Voltage level detecting circuit
- Boost circuit
- Word-line driver
- Memory array
Figure 2
Control the boost circuit based on the clock signal, the first operating voltage and a predetermined voltage

Use the boost circuit for boosting the first operating voltage to a second operating voltage

Use the second operating voltage to drive several transistors in the memory array

Figure 3
CONTROL CIRCUIT OF SRAM AND OPERATING METHOD THEREOF

BACKGROUND OF THE INVENTION

[0001] Field of the Invention: This invention relates to a memory, and particularly to a control circuit of SRAM and operating method thereof.

[0002] Description of the Prior Art

[0003] According to the operating type, the conventional memory can be divided into several categories, such as the dynamic random access memory (DRAM) and the static random access memory (SRAM). Wherein, the memory cell of the static random access memory (SRAM) is composed of a plurality of transistors, which has high switching speed and does not need any additional upgrading circuit. The so-called “static state” means when the power is applied to the static random access memory, the stored data can be kept constantly. On the contrary, the data stored in the dynamic random access memory (DRAM) has to be upconverted periodically. However, when the power supply is stopped completely, the data stored in the static random access memory will still be disappeared.

[0004] The static random access memory (SRAM) is generally applied to the products, such as the portable electronic devices, and the System-on-Chip (SOC) etc. At present, the design of common static random access memory (SRAM) comprises various types of structure, such as five-transistor structure, six-transistor structure or eight-transistor structure etc.

[0005] However, under the advanced semiconductor process, the write ability of static random access memory is relatively low, it is necessary to use more transistors to complete the memory cells of a bit, so that the unit capacity will be lower, and the power consumption will be higher. Therefore, although the word-line boost circuit is used, but its risk is that the gate oxidation layer will be easy to be penetrated.

[0006] Therefore, in order to produce more efficient static random access memory, provide better operating efficiency and lower manufacturing cost, it is necessary to research and develop the new auxiliary circuit of static random access memory.

SUMMARY OF THE INVENTION

[0007] It is an object of the present invention is to provide a control circuit of SRAM. In an embodiment, the control circuit of SRAM comprises a memory array, a word-line driver, a boost circuit, and a voltage level detecting circuit. The memory array comprises a plurality of memory cells. Each memory cell includes a plurality of transistors. The word-line driver is to activate the word-line of the memory array for cell storage memory access. The boost circuit is coupled with the word-line driver and the first operating voltage to provide the higher voltage source for the first operating voltage for boosting the first operating voltage to a second operating voltage. The voltage level detecting circuit is coupled with the first operating voltage and the DECT signal corresponding to the first operating voltage to detect the operating of the boost circuit based on the detecting-trigger signal, the first operating voltage, and the predeterminated voltage.

[0008] In an embodiment, if the first operating voltage is smaller than the predeterminated voltage, the voltage level detecting circuit will activate the boost circuit. If the first operating voltage is greater than the predeterminated voltage, the voltage level detecting circuit will control the boost circuit for stopping the boost treatment of the first operating voltage.

[0009] In an embodiment, the voltage level detecting circuit also includes a reference unit and a detecting unit. The reference unit has a first node. The detecting unit has a second node. The voltage of the first node equals to the voltage of the second node when detecting.

[0010] In an embodiment, the voltage level detecting circuit also includes a reference unit, which is coupled with the first operating voltage and the detecting unit.

[0011] In an embodiment, the voltage level detecting circuit also includes a first inverter and a first transistor reference unit. The first inverter is coupled with the DECT signal. The first transistor is coupled with the output terminal, the ground terminal of the first inverter and the detecting unit.

[0012] In an embodiment, the detecting unit also includes a second inverter and a third inverter. The detecting unit is coupled with the reference unit, the DECT signal and the fourth inverter.

[0013] In an embodiment, the operating method for the control circuit of SRAM includes controlling the operating of the boost circuit based on the DECT signal, the first operating voltage and the predeterminated voltage; using the boost circuit to boost the first operating voltage to a second operating voltage; and using the second operating voltage to drive several transistors in the memory array.

[0014] In an embodiment, if the first operating voltage is smaller than the predeterminated voltage, the boost circuit will be controlled for boosting the first operating voltage to a second operating voltage.

[0015] In an embodiment, if the first operating voltage is greater than the predeterminated voltage, the boost circuit will be controlled for stopping the boost treatment of the first operating voltage.

[0016] In comparison with the prior art, the control circuit and its operating method of the present invention uses the voltage level detecting circuit to detect whether the operating voltage (V_L) is greater than the predeterminated voltage. If the operating voltage is greater than the predeterminated voltage, the boost circuit will be shut down. If the operating voltage is smaller than the predeterminated voltage, the boost circuit will be activated. In this kind of circuit design, the fault tolerance will be higher, and the gate oxidation layer of transistor in the memory cell will not be penetrated due to the boost circuit.

[0017] Therefore, the advantage and spirit of the present invention can be understood further by the following detailed description of invention and attached Figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

[0019] FIG. 1 shows a block diagram in accordance with an embodiment of the present invention.

[0020] FIG. 2 shows the circuit of the voltage level detecting circuit in accordance with an embodiment of the present invention.

[0021] FIG. 3 shows the operating method for the control circuit of SRAM in accordance with the present invention.
DESCRIPTION OF THE PREFERRED EMBODIMENT

[0022] FIG. 1 shows a block diagram in accordance with an embodiment of the present invention. The control circuit 1 of SRAM in accordance with an embodiment the present invention includes a voltage level detecting circuit 11, a boost circuit 12, a word-line driver 13 and a memory array 14.

[0023] The voltage level detecting circuit 11 of the present invention shown in FIG. 1 is coupled with the operating voltage \( V_{DD} \) (not shown in the Figure), the ground terminal (not shown in the Figure) and the boost circuit 12. The boost circuit 12 is coupled with the operating voltage \( V_{DD} \) (not shown in the Figure) and the word-line driver 13. The word-line driver 13 is coupled with the memory array 14. The word-line driver 13 is to activate the word-line of the memory array 14 for cell storage data access. In the present invention, the memory array 13 is SRAM type memory, which may adopt 5 transistors, 6 transistors or 8 transistors, but not limited by this. The boost circuit 12 is to provide the higher voltage source for the word-line driver 13 and a first operating voltage for boosting the first operating voltage to become a second operating voltage.

[0024] FIG. 2 shows the circuit of the voltage level detecting circuit in accordance with an embodiment of the present invention. The voltage level detecting circuit 11 is detecting if the first operating voltage \( V_{DD} \) needed to be boosted with boost-operation and a DECT signal and controls the operating of the boost circuit based on the first operating voltage \( V_{DD} \) and a predetermined voltage. The voltage level detecting circuit 11 shown in FIG. 2 comprises a reference unit 111, a detecting unit 112, a first inverter 113, a first transistor M1, and a second inverter 114. The reference unit 111 also comprises a resistor R and a second transistor M2. The detecting unit 112 also comprises a first transistor pair 1123, a second transistor pair 1124, a third inverter 1121 and a fourth inverter 1122.

[0025] In the embodiment of FIG. 2, the reference unit 111 provides a reference voltage based on the operating voltage \( V_{DD} \) to the detecting unit 112 in this embodiment. In this embodiment, the second transistor M2 is a P-type Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), but not limited by this. One terminal of the resistor R of the reference unit 111 is coupled with the operating voltage \( V_{DD} \). Another terminal of the resistor R of the reference unit 111 is coupled with the source of the second transistor M2. In addition, a first node ST1 is located between the resistor R and the second transistor M2. The gate of the second transistor M2 is connected with the drain of the second transistor M2.

[0026] In the embodiment of FIG. 2, the detecting unit 112 is coupled with the reference unit 111, the gate of the first transistor, the output terminal of the first inverter 113, and the input terminal of the second inverter 114. The first transistor M1 an N-type Metal-Oxide-Semiconductor Field-Effect Transistor, but not limited by this. The input terminal of the first inverter 113 is used to receive a detecting-trigger signal DECT. The output terminal of the first inverter 113 is coupled with the gate of the first transistor M1. The drain of the first transistor M1 is coupled with the drain of the second transistor M2. The source of the first transistor M1 is grounded.

[0027] In the embodiment of FIG. 2, the first transistor pair 1123 comprises a P-type Metal-Oxide-Semiconductor Field-Effect Transistor and an N-type Metal-Oxide-Semiconductor Field-Effect Transistor. The second transistor pair 1124 also comprises a P-type Metal-Oxide-Semiconductor Field-Effect Transistor and an N-type Metal-Oxide-Semiconductor Field-Effect Transistor. The gate of P-type MOS transistor of the first transistor pair 1123 and the gate of N-type transistor of the second transistor pair 1124 receive the detecting-trigger signal DECT. The gate of N-type MOS transistor of the first transistor pair 1123 and the gate of P-type transistor of the second transistor pair 1124 are coupled with the output terminal of the first inverter 113 to receive an inverted detecting-trigger signal. The first transistor pair is also coupled with the first node ST1.

[0028] In addition, a second node ST2 is located between the first transistor pair 1123 and the second transistor pair 1124 of the detecting unit 112 shown in FIG. 2. The voltage level of the first node ST1 and the second node ST2 is the same in this embodiment when is in detecting state with DECT low, and then after detecting already with a high DECT, the detecting unit locks the detecting signal and judges whether detecting or not.

[0029] However, in the other embodiment, the voltage level of the first node ST1 and the second node ST2 might be slightly different. In the detecting unit 112 of this embodiment, the input terminal of the third inverter 1121 is coupled with the second node ST2, the input terminal of the fourth inverter 1122 is coupled with the output terminal of the third inverter 1121, and the output terminal of the fourth inverter 1122 is coupled with the second transistor pair 1124. In addition, the input terminal of the second inverter 114 of the voltage level reference circuit 111 is coupled with the output terminal of the third inverter 1121 and the input terminal of the fourth inverter 1122. The output terminal of the second inverter 114 is coupled with the boost circuit 12 to control the operating of the boost circuit 12.

[0030] FIG. 3 shows the operating method for the control circuit of SRAM in accordance with the present invention. Please refer to FIG. 1 and FIG. 2 for its description. In Step S305, the voltage level detecting circuit 1 controls the operating of the boost circuit 12 based on the detecting-trigger signal DECT, the operating voltage \( V_{DD} \), and a predetermined voltage. In this embodiment, the predetermined voltage may be the trigger point of the third inverter 1121. The Step S305 will be further described as follows. When the first transistor pair 1123 is activated, the voltage of first node ST1 equals to the voltage of second node ST2. Actually, the voltage level reference unit 111 controls the first transistor M1, the second transistor M2 and the detecting unit 112 based on the detecting-trigger signal DECT, and further compares the voltage of first node ST1 and the trigger point of the third inverter 1121, and then outputs a control signal to the boost circuit 12 through the second inverter 114.

[0031] In FIG. 3, if the operating voltage \( V_{DD} \) is greater than the predetermined voltage through M2 current source due to voltage change ST1 of the resistor R, the voltage level detecting circuit 11 will control the boost circuit 12 for stopping the boost treatment of the operating voltage \( V_{DD} \). If the operating voltage ST1 is smaller than the predetermined voltage, the voltage level detecting circuit will activate the boost circuit 12 by the control signal.

[0032] In Step S310 of FIG. 3, when the voltage level detecting circuit 11 activates the boost circuit 12 by the control signal, the boost circuit 12 will boost the operating voltage \( V_{DD} \) to another operating voltage \( V_{DD} \) based on the abovementioned control signal. When the voltage level detecting circuit 11 stops the operating of the boost circuit 12, the boost circuit 12 will stop the boost treatment, so that the
output voltage provided by the boost circuit 12 will not penetrate the gate oxidation layer, especially under high voltage operation.

[0033] In Step S315 of FIG. 3, the word-line driver 13 uses the operating voltage $V_{\text{DD}}$ treated by the boost circuit 12 to drive several transistors in the memory array 14.

[0034] In comparison with the prior art, the embodiment of the present invention uses simple digital circuit to judge whether the operating voltage $V_{\text{DD}}$ is greater than a predetermined voltage, in order to determine the operating of the boost circuit. The circuit of the present invention copes with the word-line driver to get higher fault tolerance and can avoid penetrating the gate oxidation layer, in order to raise the operating efficiency of SRAM and reduce the manufacturing cost of SRAM.

[0035] It is understood that various other modifications will be apparent to and can be readily made by those skilled in the art without departing from the scope and spirit of this invention. Accordingly, it is not intended that the scope of the claims appended hereto be limited to the description as set forth herein, but rather that the claims be construed as encompassing all the features of protential novelty that reside in the present invention, including all features that would be treated as equivalents thereof by those skilled in the art to which this invention pertains.

What is claimed is:

1. A control circuit of SRAM, comprising:
   a memory array means for having a plurality of memory cells, each said memory cell having a plurality of transistors;
   a word-line driver means for activating a word-line of said memory array for cell storage data accessing;
   a boost circuit means for coupling with said word-line driver and a first operating voltage to provide a higher voltage source for said first operating voltage for boosting said first operating voltage to become a second operating voltage; and
   a voltage level detecting circuit means for coupling with said first operating voltage and a detecting-trigger signal to control said operating of said boost circuit based on said detecting-trigger signal, said first operating voltage and a predetermined voltage.

2. The control circuit according to claim 1, wherein if the first operating voltage is greater than the predetermined voltage, the voltage level detecting circuit controls the boost circuit for stopping the boost treatment of the first operating voltage, and if the first operating voltage is smaller than the predetermined voltage, the voltage level detecting circuit activates the boost circuit.

3. The control circuit according to claim 1, wherein the voltage level detecting circuit further comprises a reference unit and a detecting unit; the reference unit has a first node, the detecting unit having a second node, and the voltage of the first node equals to the voltage of the second node while detecting with a low DECT, and then after detecting already with a high DECT, the detecting unit locks the detecting signal and judges whether detecting or not.

4. The control circuit according to claim 1, wherein the voltage level detecting circuit further comprises a reference unit, said reference unit is coupled with the first operating voltage and the detecting unit.

5. The control circuit according to claim 4, wherein the voltage level detecting circuit further comprises a first inverter and a first transistor reference unit, the first inverter is coupled with the detecting-trigger signal, and the first transistor is coupled with the output terminal, the ground terminal of the first inverter and the detecting unit.

6. The control circuit according to claim 4, wherein the detecting unit further comprises a second inverter and a third inverter, the detecting unit is coupled with the reference unit, the detecting-trigger signal and the fourth inverter.

7. An operating method for the control circuit of SRAM, comprising:
   controlling the operation of a boost circuit based on a detecting-trigger signal, a first operating voltage and a predetermined voltage;
   using the boost circuit to boost the first operating voltage to become a second operating voltage; and
   using the second operating voltage to drive several transistors in a memory array.

8. The operating method according to claim 7, wherein based on the detecting-trigger signal, the first operating voltage and the predetermined voltage, if the first operating voltage is smaller than the predetermined voltage, the boost circuit is controlled for boosting the first operating voltage to become a second operating voltage.

9. The operating method according to claim 7, wherein based on the detecting-trigger signal, the first operating voltage and the predetermined voltage, if the first operating voltage is greater than the predetermined voltage, the boost circuit is controlled for stopping the boost treatment of the first operating voltage.