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Formation of Ge nanocrystals using Si$_{1.33}$Ge$_{0.67}$O$_2$ and Si$_{2.67}$Ge$_{1.33}$N$_2$ film for nonvolatile memory application

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The authors proposed a formation mechanism of Ge nanocrystals embedded in the dielectric by using Si$_{1.33}$Ge$_{0.67}$O$_2$ and Si$_{2.67}$Ge$_{1.33}$N$_2$ films for nonvolatile memory application in this study. Because of internal competition reaction, this formation process reduced the thermal budget and eliminated the use of high pressure H$_2$ treatment or steam process. In this research, the preannealing capping oxide step is a critical process for nonvolatile memory effect. Transmission electron microscope shows the shape and density of nanocrystals in the dielectric. Moreover, the memory structure with Ge nanocrystal embedded in SiN$_x$ has better charge storage ability and data retention than Ge nanocrystal embedded in SiO$_x$. © 2007 American Institute of Physics. [DOI: 10.1063/1.2779931]

The nonvolatile memory (NVM) for portable electronic productions is an important industrial semiconductor because of its superiority in low-power consumption, low cost, high-memory capacity, and enough data retention. The conventional NVM with floating gate (FG) structure, however, cannot efficaciously prevent data loss in terms of reliability trials for future scaling down process. Due to the discrete charge storage nodes acting as charge trapping layer to reform drawbacks of conventional FG memory, the NVMs using various semiconductor nanocrystals have been widely investigated in the past few years, such as silicon (Si), germanium (Ge), and zinc oxide (ZnO) nanocrystals. Moreover, the Ge nanocrystal has better memory performance than Si and ZnO nanocrystals because of its smaller energy band gap (~0.6 eV) and higher dielectric constant (~16.0, i.e., stronger coupling with the conduction channel). According to the current research, the self-assembled and direct growth of Ge nanocrystals embedded in SiO$_2$ layer has successfully been implemented. The self-assembled method was reported by many previous studies because it could control better density and size of nanocrystals than direct growth. Nevertheless, the self-assembled method must need a high temperature (~900–1100 °C) with long duration (~30–60 min) oxidation process to anneal the charge trapping layer which is generally deposited by various ratios of SiGe layer, and an overoxidation phenomenon of Ge nanocrystals is often obtained after foregoing oxidation process. Hence, a redox step must be added to the formation flow of Ge nanocrystal by using an additional high pressure H$_2$ treatment or steam process.

We therefore undertook a different line of investigation to shun the disadvantages of self-assembled method and reduce thermal budget. Our investigation focused on the use of silicon-germanium oxide (SiGeO) and silicon-germanium nitride (SiGeN) thin films to form high density and good spatial distribution of Ge nanocrystals embedded in the dielectric for NVM application. In this letter, we also found that preannealing capping oxide (PACO) was a critical step for formation and electronic characteristics of Ge nanocrystals. The fabrication of NVM structure was started with a thermal dry oxidation at 950 °C to form a tunnel oxide about 5 nm on p-type (100) Si wafer which had been removed native oxide and particles by RCA process, and then a 10-nm-thick charge tapping layer was deposited by reactive sputtering of SiGeO$_{x}$ target in the Ar/O$_2$ [24/2 SCCM (SCCM denotes cubic centimeter per minute at STP)] ambiance at room temperature. This step could obtain a Si$_{1.33}$Ge$_{0.67}$O$_2$ layer which the ratio of atom concentration was analyzed by x-ray photoelectron spectroscopy. Besides, we used nitrogen (N$_2$, 20 SCCM) to act for O$_2$ to form Si$_{2.67}$Ge$_{1.33}$N$_2$ layer during sputtering process in order to lead in nitride improved charge storage ability. Before rapid thermal annealing (RTA) process at 900 °C for 30 s in the N$_2$ ambiance, the Si$_{1.33}$Ge$_{0.67}$O$_2$ and Si$_{2.67}$Ge$_{1.33}$N$_2$ layers must be capped by a 20-nm-thick oxide using a plasma enhanced chemical vapor deposition (PECVD) system at 300 °C (this step was called PACO). The RTA process was performed to cause the self-assembly of Ge nanocrystal in the charge trapping layer. After RTA process, a 20-nm-thick blocking oxide was deposited by PECVD and then deposited Al gate electrodes to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure. Transmission electron microscope (TEM) analysis was assumed for microstructure of Ge nanocrystals. Electrical characteristics of the capacitance-voltage (C-V) hysteresis were also measured by HP4284 precision LCR meter with high frequency of 1 MHz. Figure 1 shows the electrical characteristics of C-V hysteresis under ±10 gate voltage operation with (1) Ge nanocrystal embedded in SiO$_x$ (use of PACO step), (2) Ge nanocrystal embedded in Si$_{1.33}$Ge$_{0.67}$O$_2$ (use of PACO step), (3) Ge nanocrystal embedded in Si$_{2.67}$Ge$_{1.33}$N$_2$ (use of PACO step), and (4) silicon nanocrystal embedded in SiO$_x$ (without PACO step). The LCR meter was used to measure the different capacitance and resistance of each sample in the ±10 gate voltage operation with a high frequency of 1 MHz.
better charge storage ability. From Fig. 1 higher Ge concentration in the charge trapping layer to get the PACO step to avoid Ge atom outdiffusion and keep PACO step formation of Ge nanocrystals, the Gibbs free energy of Si–O compared with Ge–O, the oxygen atoms can interact with Si atom easier than with Ge atom in the Si1.33Ge0.67O2 layer during the RTA process. It can be considered that an internal competition reaction will induce self-assembled of Ge nanocrystals in the Si1.33Ge0.67O2 layer, which is dependent on the amount of oxygen of charge trapping layer. Therefore, Ge nanocrystals could be formed at lower thermal budget and no use of further high pressure H2 treatment or steam process in our experimental method.

We also use the internal competition reaction for Si1.33Ge0.67N2 layer to form Ge nanocrystal embedded in SiNx, as shown in the cross-sectional TEM image of Fig. 3(b). The average diameter of the nanocrystals is approximately 7–8 nm and the area density of the nanocrystals is estimated to be about 1.12 × 1012 cm−2 by TEM analysis. For the formation of Ge nanocrystals, the Gibbs free energy of Si–O and Ge–O at 900 °C, are about −805 and −666 kJ mol−1, respectively.14 Because of the smaller Gibbs free energy of Si–O compared with Ge–O, the oxygen atoms can interact with Si atom easier than with Ge atom in the Si1.33Ge0.67O2 layer during the RTA process. It can be considered that an internal competition reaction will induce self-assembled of Ge nanocrystals in the Si1.33Ge0.67O2 layer, which is dependent on the amount of oxygen of charge trapping layer. Therefore, Ge nanocrystals could be formed at lower thermal budget and no use of further high pressure H2 treatment or steam process in our experimental method.

The retention of nonvolatile nanocrystal memory structure with (1) and (2) are illustrated in Fig. 4. The retention measurement was performed at room temperature by operating a ±15 V gate voltage stress for 10 s and measured up to

![Fig. 1. Capacitance-voltage (C-V) hysteresis of MOIOS structure under ±10 gate voltage operation with (a) (3) Ge nanocrystal embedded in SiO2, (no use of PACO step) and (b) (1) Ge nanocrystal embedded in SiO2 (use of PACO step) and (2) Ge nanocrystal embedded in SiN, (use of PACO step). PACO: preannealing capping oxide.](image1)

![Fig. 2. Secondary ion mass spectrometer (SIMS) analysis of MOIOS structure with Ge of before annealing, Ge of structure (3) (no use of PACO step), and Ge of structure (1) (use of PACO step).](image2)

![Fig. 3. Cross-sectional transmission electron microscope (TEM) analysis of MOIOS structure with (a) Ge nanocrystal embedded in SiO2, (the nanocrystal size and density are about 5–6 nm and 1.73 × 1012 cm−2, respectively) and (b) Ge nanocrystal embedded in SiN, (the nanocrystal size and density are about 7–8 nm and 1.12 × 1012 cm−2, respectively.)](image3)

![Fig. 4. Retention with structure (1) Ge nanocrystal embedded in SiO2 and structure (2) Ge nanocrystal embedded in SiN, at room temperature operating at ±15 V gate voltage stress for 10 s. The charge holding ratio of structure (1) is 7% and that of structure (2) is 20% after 106 s.](image4)
The flatband voltage shift ($\Delta V_{fb}$) was obtained by comparing the $C-V$ curves from a charged carrier state and the quasineutral state. We find that the charge holding ratio of structure 2, 20%, is better than that of structure 1, 7%, after $10^6$ s by analyzing the extrapolation value of retention data [dotted dashed line for (1) and dotted line for (2) of Fig. 4]. Because structure 2 provided trapping states of SiN$_x$ for charging carriers, this result could reduce the Coulomb blockade effect of charge trapping layer leading to lower tunneling probability between tunnel oxide and conduction channel under retention state. Hence, the nanocrystals combined with SiN$_x$ matrix can improve the performance of nonvolatile nanocrystal memory in our investigation.

In conclusion, we successfully fabricated the Ge nanocrystals embedded in the dielectric by using the self-assembled characteristics of Si$_{1.33}$Ge$_{0.67}$O$_2$ and Si$_{2.67}$Ge$_{1.33}$N$_2$, and cut down thermal budget. The overoxidation phenomenon of Ge nanocrystals could be prevented through different Gibbs free energies of compounds. The Ge nanocrystals combined with SiN$_x$ matrix showed better electronic performance for nonvolatile memory application. In addition, this fabrication technique can be compatible with current manufacturing process of the integrated circuit.

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