Nonvolatile Si $\text{Si O}_2$ Si N $\text{Si O}_2$ Si type polycrystalline silicon thin-film-transistor memory with nanowire channels for improvement of erasing characteristics

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Nonvolatile Si/SiO₂/SiN/SiO₂/Si type polycrystalline silicon thin-film-transistor memory with nanowire channels for improvement of erasing characteristics

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A silicon-oxide-nitride-oxide-silicon type polycrystalline silicon thin-film transistor (poly-Si TFT) with nanowire channels was investigated for both transistor and memory applications. The poly-Si TFT memory device has superior electrical characteristics, such as higher drain current, smaller threshold voltage, and steeper subthreshold slope. Also, the simulation result on electrical field reveals that the electrical field across the tunnel oxide is enhanced and that across the blocking oxide is reduced at the corner regions. This will lead to the parasitic gate injection activity and the erasing speed can be apparently improved in the memory device due to the pronounced corner effect and narrow channel width. © 2007 American Institute of Physics. [DOI: 10.1063/1.2798600]
A 400-nm-thick thermal oxide layer was first grown on the Si wafer by furnace system to replace a glass substrate. Then an undoped 50-nm-thick amorphous silicon (a-Si) layer was deposited on the oxidized silicon wafer by low-pressure chemical vapor deposition (LPCVD) at 550 °C. Subsequently, the deposited a-Si layer was recrystallized by solid-phase crystallization at 600 °C for 24 h under N₂ ambient. After the patterning of active region with electron beam lithography and dry etching process, the 25-nm-thick oxide-nitride-oxide (ONO) multilayer gate dielectric layers were formed by LPCVD: the 5 nm tunnel oxide (TO), 10 nm silicon nitride (SiN), and 10 nm blocking oxide (BO), sequentially. A 150-nm-thick in situ n⁺ doped poly-Si layer was then deposited and defined. After S/D formation by self-aligned phosphorous implantation, a 200 nm oxide passivation layer was deposited and contact holes were patterned. Finally, Al metallization was performed and the devices were sintered at 400 °C in nitrogen ambient for 30 min. The studied TFT devices with the same gate length of 5 μm consist of different channels in width, including ten strips of 65 nm nanowire (NW), five strips of 200 nm channels (M5), two strips of 500 nm channels (M2), and a single-channel (S1) with 1 μm.

Figure 1 presents the transfer normalized $I_D-V_G$ curves of SONOS-TFTs with various structures. Obviously, the NW device has superior performance, such as the highest drain current, smallest threshold voltage ($V_{th}$), and steepest subthreshold swing (SS). The $V_{th}$ decreases from 2.5 V to 1.7 V and SS decreases from 0.5 to 0.4 V/decade in order from the S1 structure to the NW structure. Different from the other structures, the nanowire is surrounded by the poly-Si gate to form the trigate structure, shown as the inset TEM photography. The physical width of nanowire channel is confirmed to be 65 nm and the thickness of ONO is 25 nm. Since the

![FIG. 1. Comparison of typical $I_D-V_G$ characteristics of the SONOS-TFTs with various structures. The inset exhibits the transmission electron microscopy (TEM) of a single nanowire channel of NW SONOS-TFT.](image1)

The physical width of nanowire channel is confirmed to be 65 nm and the thickness of ONO is 25 nm. Since the effective channel width is increased by the trigate structure, the drain current can be improved in NW SONOS-TFT. To study the electrical improvement for the subthreshold behavior, the distribution of electrical field across the stacked gate dielectric of nanowire channel were numerically simulated at a gate bias of 2 V ($~V_{th}$) by ISE-TCAD simulator, as shown in Fig. 2. It can be seen that the electrical field near the SiO$_2$/poly-Si interface at corner region is very high. This will lead the current at the corner region to turn on earlier than that at the noncorner region due to the corner effect induced electrical field. The corner current can provide major current as the device operated in subthreshold region. Thus, the corner effect plays a dominant role to enhance the subthreshold behavior.

The SONOS-TFTs also can act as a nonvolatile memory by using the nitride layer as a charge trapping layer, in addition to transistor application. Figure 3 shows the $I_D-V_G$ curves of device before and after the programing/erasing operations by FN tunneling scheme. The results reveal that the threshold voltage of a fresh memory device is different from those of the memory device after erasing operation. Because the electrons will inject to silicon nitride layer from the control gate via FN tunneling, it is difficult for the SONOS-TFT memory to return to the original state of threshold voltage after performing an erase procedure.

![FIG. 2. Simulation of the electrical fields with a gate bias of 2 V in nanowire at corner and noncorner regions.](image2)

![FIG. 3. The $I_D-V_G$ curves of device before memory operation (fresh) and after the programing/erasing operations. The program and erase conditions are 16 V for 100 μs and −18 V for 10 s, respectively.](image3)
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