The Analysis and Design of CMOS Current-Mode RF Receiver Front-End Integrated Circuits

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The Analysis and Design of CMOS Current-Mode RF Receiver Front-End Integrated Circuits

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互補式金氧半電流操作模式之射頻接收器前端電路設計與分析

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摘要

在這篇論文中，描述了低電壓、電流模式毫米波射頻前端電路的設計法及實現技巧。本篇論文主要分三個部份，包含了 (1) 利用電容回授的匹配網路技巧，來模組化、設計、以及分析低雜訊放大器；(2) 低LO功率、三十度相位差、平衡架構，自行開關(self-switching)的電流模式混頻器的設計與分析；(3) 設計與分析一個擁有在兩百四十億赫茲的單晶片LO訊號產生器，以及直流偏移補償的1伏特電流模式接收機前端電路。

首先，一個針對於低雜訊放大器的新的輸入阻抗功率匹配技巧被提出。在所提出的技巧中，輸入共源極放大器的開極-汲極電容及電容回授匹配網路被用來實現一個實數的輸入阻抗，以至於能和輸入源極阻抗匹配。使用這個技巧，能同時達到雜訊最小與功率增益最大，並且能在不耗損線性度下使用非常低的電源電壓。所提出的低雜訊放大器的雜訊分析由數學推導以及量測結果互相佐證。在此所提出之13GHz低雜訊放大器使用0.18μm 1P6M金氧半製程技術實現。在量測結果上，增益(S21)為13.2分貝，雜訊指數(noise figure)為4.57分貝，以及最低雜訊指數(Fmin)為4.46分貝。此低雜訊放大器之隔絕(reverse isolation)可達-40分貝，在輸入及輸出阻抗匹配接低於-11分貝。在線性度部份，增益1分貝壓縮點為-11 dBm 與 三階互調失真點為-0.5 dBm。在供應電壓1伏特時低雜訊放大器之電流消耗為10mA。
其次，提出了一個毫米波射頻河補型金氧半、低 LO 功率、九十度相位差、平衡架構、自行開關(self-switching)的電流模式混頻器。此混頻器的組成，由一個輸入級的共開極放大器、一個省面積的九十度分支線混合耦合器，以及金氧半自行開關(self-switching)的裝置。90 度分支線混合耦合器被設計來處理在非常高頻上的射頻與 LO 訊號的結合。為了實現省面積的90度分支線混合耦合器，基於並聯電容的高阻抗耦合器波導，分支線及 through-line 由原來的四分之波長各自減少為六點四分之波長與十分之波長。所提出之混波器使用 0.13–μm 1P8M 金氧半製程技術實現。在 58GHz 功率為 0dBm 之 LO 訊號下，能將 60–GHz 射頻訊號降至 2–GHz 中頻訊號。在這次設計中，此混波器之單端轉換增益(single-end conversion gain)為 1 分貝，其輸入增益 1 分貝壓縮點為 2 dBm。LO 與 RF 訊號隔絕可達到–37 分貝，在供應電壓 1.2 伏時其電流消耗為 3mA。

最後，在此發表工業-科學-醫學接收器操作在 24GHz。此接收機由一個低雜訊放大器、射頻混頻器、IF 混頻器，直流偏移補償、電壓控制振盪器，以及一個除二電路。在論文第一部份所提及的低雜訊放大器，在貢獻最小的雜訊下用來放大在兩百四十億赫茲的射頻訊號，以增大接收訊號與雜訊間的差距。被增大的兩百四十億赫茲的射頻輸入訊號再經由論文第二部份所提及的射頻混頻器降頻至八十億赫茲的 IF 頻段。隨後的 IF 混頻器分成等相位與九十度相位差兩條路徑，把 IF 頻率直接降頻至零。此兩基頻訊號再利用直流偏移補償電路來消除在 IF 混頻器輸出端由 LO 自身混頻所產生的直流偏移。所提出之接收器使用 0.13–μm 1P8M 金氧半製程技術實現，此接收器之增益為 19.5 分貝、雜訊指數為 15 分貝與輸入阻抗匹配(S11)皆低於–13 分貝。其輸入增益 1 分貝壓縮點為–25dBm。在供應電壓 1 伏特時其電流消耗為 35mA。
所提出的射頻電路及接收機前端電路相信能適用於設計高頻、高效能、低電壓、高整合度、全金氧半的毫米波無線通訊系統。在未來會在收發機上做更進一步的研究。
ABSTRACT

In this thesis, the design methodologies and implementation techniques of low-voltage current-mode high-frequency RF front-end circuits are presented. There are three parts in this thesis, including (1) the modeling, design, and analysis of low-noise amplifier utilizing the technique of capacitive feedback matching network; (2) the design and analysis of low LO-power quadrature balanced self-switching current-mode mixer; (3) the design and analysis of a 1-V current-mode front-end receiver with on-chip LO signal generator and DC-offset compensation circuit at 24-GHz RF application.

At first, a new input impedance power matching technique for LNA is proposed and analyzed. In the proposed technique, the gate-drain capacitor of the input common-source amplifier and the capacitive feedback matching network are used to implement a real input impedance in order to match with the input source impedance. Thus the technique is called technique of capacitive feedback matching network. By using this technique, the minimum noise figure and maximum power gain can be
achieve simultaneously, furthermore, it can be used with very low supply voltage without degraded the linearity. The full noise analysis of LNA utilizing the proposed technique is supported by mathematical derivations and it is complemented and validated by measurements. Where, the proposed LNA which is implemented in a 0.18-μm 1P6M CMOS technology is operated at the frequency of 13 GHz. It has a gain $S_{21}$ of 13.2 dB, a noise figure (NF) of 4.57 dB and an $NF_{\text{min}}$ of 4.46 dB. The reverse isolation $S_{12}$ of the LNA can achieve $-40$ dB and the input and output return losses are better than $-11$ dB. The input 1-dB compression point is $-11$ dBm and IIP3 is $-0.5$ dBm. This LNA drains 10 mA from the supply voltage of 1 V.

Secondly, mm-wave RF CMOS low LO-power quadrature balanced self-switching current-mode mixer is proposed. The mixer consists of common-gate amplifier as input stage, an area efficient 90-degree branch-line hybrid coupler, and CMOS self-switching current-mode devices, the 90-degree branch-line hybrid coupler is designed to deal with the issue on the combination of RF and LO signals at very high frequency, in order to implement area efficient 90-degree branch-line hybrid coupler, the branch-line and the through-line lengths of the hybrid are reduced from lambda/4 to lambda/6.4 and lambda/10, respectively, based on the methodology of a high-impedance coplanar waveguide with shunt lumped capacitors. The proposed mixer, using 0.13-μm 1P8M CMOS technology, can down-convert 60-GHz RF signal to 2-GHz intermediate frequency (IF) signal, with a LO power of 0 dBm at 58 GHz. In the design, the mixer had a single-end conversion gain of 1dB and an input-referred 1dB compression point of 2 dBm. The LO-RF isolation of the mixer can achieve $-37$ dB while using 3 mA from a supply voltage of 1.2V.

Finally, Industrial-Science-Medical (ISM) receiver operates at 24 GHz is proposed. The receiver consists of transconductance low-noise amplifier (TLNA), RF current-mode mixer, IF current-mode mixers, DC-offset compensation, voltage control oscillator (VCO), and quadrature divided-by-two circuit (QD2). The TLNA proposed in
the first part of the thesis is used to amplified the RF input spectrum at 24 GHz with minimal noise contribution to enlarge the power difference between the received signal and noise, then the amplified RF input spectrum at 24 GHz is down-converted to an intermediate frequency (IF) of 8 GHz by using RF current-mode mixer proposed in the second part of the thesis, and a follow-up IF current-mode mixers are used in-phase I and quadrature Q paths to directly convert the spectrum at IF frequency to zero frequency. The baseband signals are then applied to the DC-offset compensation circuit to eliminate DC-offset currents appear at the output of the IF current-mode mixer due to the self-mixing of the LO. The fabricated circuit in 0.13–μm 1P8M CMOS technology demonstrates a conversion gain of 19.5 dB, and noise figure of 15 dB, while maintaining an input return loss better than −13-dB. The input-referred 1dB compression point of −25 dBm is measured. This receiver drains 35 mA from the supply voltage of 1 V.

It is believed that the proposed RF circuits and receiver front-end can be applied to the design of high-frequency high-performance low-voltage high-integration all-CMOS wireless communication systems. Future research on transceiver components will be conducted in the future.
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To My Dear Family & Friends

“I saw that no man writes a book in his day but said in a next day: if this was changed, it will be good. If this was added, it will be better. If this was forward it will be the best. If this was left, it will beautiful. This is the eloquent proof, which is evidence of the shortage of human beings.”
# Table of Contents

ABSTRACT (CHINESE) ii

ABSTRACT (ENGLISH) v

ACKNOWLEDGEMENTS viii

Table of Contents x

List of Tables xii

List of Figures xiii

1 INTRODUCTION 1

1.1 Background ................................... 1

1.2 Research Motivation .............................. 3

1.3 Organization Of This Thesis ...................... 4

List of Symbols 1

2 REVIEWS ON FRONT- END RECEIVERS, LOW-NOISE AMPLIFIERS, AND MIXERS 10

2.1 Receiver Architectures ........................................ 11

2.1.1 Homodyne, Direct- Conversion, or Zero- IF Receiver ............. 11

2.1.2 Heterodyne or IF Receivers .......................... 11

2.1.3 Image- Reject Receiver ........................... 13

2.1.4 Wideband- IF Receiver .......................... 14

2.1.5 Low- IF Receiver .................................. 14

2.1.6 Double- Quadrature Receiver .................. 15

2.2 CMOS Low-Noise Amplifiers .............................. 17

2.3 CMOS Mixers ............................................. 19
List of Tables

2.1 Comparison of receiver architecture. ........................................... 22
2.2 Summary of recent CMOS LNA results. ................................. 23
2.3 Summary of recent high-frequency CMOS mixer results. .......... 24

3.1 The measured performance parameters of the fabricated LNA and comparisons with other published LNAs. ...................... 56

4.1 The performance summaries of the proposed mixer and comparisons with other published mixers. ............................. 73

5.1 The measured performances and comparisons results of published 24-GHz receiver front-end circuits. .............................. 93
List of Figures

1.1 Wireless communication landscape. ........................................ 6
1.2 The unlicensed bandwidth available at 60 GHz. ........................... 7
1.3 The scenarios for short-range and long-range backbone wireless communication networks for home-RF applications. ...................... 8
1.4 The reduction of supply voltage and threshold voltage in accordance with the scaling of channel length of CMOS technologies. .............. 9

2.1 The block diagram of the homodyne, direct-conversion, or zero-IF receiver. 25
2.2 Two sources of DC offsets in the direct-conversion receiver. .............. 26
2.3 The block diagram of the heterodyne or IF receiver. ...................... 27
2.4 The block diagram of the Hartley receiver. ................................ 28
2.5 The block diagram of the Weaver receiver. ................................ 29
2.6 The block diagram of the wideband-IF receiver. ........................... 30
2.7 The block diagram of the low-IF receiver. .................................. 31
2.8 Spectra flow of the low-IF receiver. ........................................ 32
2.9 The block diagram of the double-quadrature receiver. .................... 33
2.10 Spectra flow of the double-quadrature receiver. ........................... 34
2.11 a) The common-source amplifier as the input stage, b) The common-source amplifier with source degeneration inductor. .................. 35
2.12 The schematic diagram of 3-stage common-source LNA. .................. 36
2.13 The schematic diagram of cascode LNA. .................................... 37
2.14 The schematic diagram of Common-gate with resistive feedback (CGRF)LNA. 38
2.15 The schematic diagram of single-balanced mixer Gilbert cell mixer. .... 39
2.16 The schematic diagram of single-balanced mixer with current bleeding. .. 40
2.17 The schematic diagram of Cascade mixer. .................................. 41
2.18 The schematic diagram of transconductance mixer. ....................... 42
2.19 The schematic diagram of transconductance quadrature balanced mixer with hybrid combiner. .............................................. 43
2.20 The schematic diagram of drain-pumped resistive mixer. ................ 44
2.21 The schematic diagram of gate-pumped resistive mixer. .................. 45
2.22 The schematic diagram of resistive mixer. .................................. 46

3.1 The common-source amplifier as the input stage. ......................... 57
3.2 The small-signal equivalent circuit for noise calculations. ............... 58
3.3 The design steps for capacitive feedback matching network LNA. ....... 59
3.4 The complete circuit diagram of proposed LNA. ............................. 60
3.5 The measured and simulated $S_{11}$ and $S_{21}$ results of the proposed LNA. 61
3.6 The measured and simulated $S_{22}$ and $S_{12}$ results of the proposed LNA. 62
3.7 The measured stability K-factor and B-factor of the proposed LNA. .... 63
3.8 The measured and simulated noise figure $NF$ and minimum noise figure $NF_{\text{min}}$ of the proposed LNA. .................. 64
3.9 The LNA measurement results of $P_{\text{in}}$ versus $P_{\text{out}}$. ................. 65
3.10 The LNA measurement results of two-tone test. ............................. 66
3.11 The chip photograph of the proposed LNA utilizing the technique of capacitive feedback network. .............................. 67

4.1 The circuit diagram of self-switching current-mode mixer. ................. 74
4.2 The 4m+1-point analysis applied on HSPICE simulated of ac current gain. 75
4.3 Circuit diagram of CMOS quadrature balanced current-mode mixer. ...... 76
4.4 (a) Quarter-wavelength transmission line; (b) Shorted transmission line equivalent to the quarter-wavelength transmission line; (c) Coplanar waveguide. 77
4.5 The chip photograph of fabricated current-mode quadrature balanced down-conversion mixer. .......................... 78
4.6 The measurement setup for the diagram 60 GHz down-conversion mixer setup. 79
4.7 The measured and simulated IF output power versus RF input power. .... 80
4.8 The measured and simulated conversion gain versus LO power. .......... 81
4.9 The measured LO-RF isolation characteristics. ............................... 82

5.1 The block diagram of the 24-GHz current-mode receiver front-end. ....... 94
5.2 The circuit diagram of the TLNA. ............................................. 95
5.3 The simplified circuit diagram of the self-switching current-mode RF current-mode mixer. ................................. 96
5.4 The circuit diagram of the double-balance self-switching current-mode RF current-mode mixer. ............................... 97
5.5 The simulated gain of TLNA with and without notch filter. ................ 98
5.6 The circuit diagram of the quadrature IF current-mode mixers. .......... 99
5.7 The circuit diagram of DC-offset compensation circuit. .................. 100
5.8 The sensitivity of the rectifier circuit to the variation of the M52 width... 101
5.9 The circuit diagram of VCO with quadrature divided-by-two circuit. ... 102
5.10 The interconnections within the circuits in the receiver are simulated by HFSS. 103
5.11 The chip micrograph of the fabricated current-mode receiver front-end. ... 104
5.12 The measured and simulated input reflection coefficient of the proposed receiver. ................................................................. 105
5.13 The measured gain and $NF$ of the proposed receiver. .................. 106
5.14 The receiver measurement results of $P_{in}$ versus $P_{out}$. ............... 107
5.15 The measured and simulated tuning range of the VCO. .................. 108
5.16 The microphotograph of the VCO and quadrature divided-by-two circuits after laser-cut. ...................................................... 109
6.1 National Chiao Tung University on-waver probe analytical station test setup 2008. ................................................................. 114
Chapter 1

INTRODUCTION

1.1 Background

In the late of 1990s, wireless communications represent a major step forward in the dramatic story that began ten years earlier with the arrival of cellular and cordless telephones. When people spend billions of dollars to buy and use these new kinds of telephones, they demonstrate a strong desire to control their information. Mobility is at the heart of wireless communications, people transmit and receive information wherever they are and whenever they choose, even when they are moving. They want to produce and acquire information in formats they choose, including sounds, text, still pictures, moving pictures, keyboard operations, mouse movements, and pen strokes. The promise of wireless communications is to make all kinds of information available anywhere, anytime, at low cost to a large mobile population.

Although this promise has widespread appeal, practical systems that deliver it remain several years in the future. At the moment, Bluetooth, HiperLAN, HiperLAN/2, Wireless Personal Area Network (WPAN), Wireless Local Area Network (WLAN), Ultra-Wideband (UWB), WiMAX, etc. have a collection of services, each capable of performing some of the goals of the wireless communications. However, to achieve the aforementioned goals, this needs access network with very high capacity. High data-rate requires broad frequency bands, and a sufficiently broadband spectrum can be obtained in the high GHz regime (> 10 GHz) such as 24 GHz (K–Band) and 60 GHz (V–Band) as shown in Fig. 1.1. The high GHz regime offers several advantages.
1. Providing in general high bandwidth and clean RF spectrum with low cost. For example, the Federal Communications Commission (FCC) has allocated the 24-GHz frequency band for unlicensed industrial, scientific, and medical (ISM) application. Where for the 60-GHz frequency band is largely globally available, and a large amount of spectrum is available on an unlicensed basis in many regulatory domains as shown in Fig. 3.5.

2. Large spectral capacity and compact benefits of reduced co-channel interference providing dense, short reach (1 km) wireless communication due to shorter cell re-use distance [1], as well as access to worldwide allocated nonregulatory frequency bands [2].

3. Supporting system-on-chip designs. With the high-frequency of operation, passive components such as transmission lines, RF combiner, passive filters, and even antennas, can be efficiently implemented on chip [3–12].

Fig. 1.3 shows such scenarios with clusters for short ranges and a long range backbone wireless communication networks for home-RF applications at 17 GHz, 24 GHz, and 60 GHz in the near future. Although the standardizations of both applications have not been accomplished, the possibilities of new mass wireless market lead to the interest of the communication industries.

To implement new hardware for wireless communication systems, low manufacturing costs are of paramount importance to be competitive in the stringent wireless markets. Thus, the goal of the designers of personal wireless communicational devises is to design a low cost communicational device with high performance. To reach this goal, highly integrated semiconductor chips must be design, so both of the analog RF front-end and the digital baseband signal processing should be design on the same die without any external components. Due to their high unit current gain frequency ($f_T$) and maximum operating (or oscillation) frequency ($f_{max}$) SiGe(C), BiCMOS, and III-V technologies are used to realize analog RF front-end circuits. However, these technologies suffer from high cost and great difficulties to integrate with complex digital systems which are usually realized by CMOS technologies. Driven by the development trend of highly integrated semiconductor chips for wireless communication system, research on the CMOS RF front-end has accelerated.
With the continual scaling down of CMOS technology, a transit frequency \( f_T \) of up to 400GHz has been reported in sub-10nm technology nodes [13]. As a result, the CMOS technology has become a potential choice for the implementation of high-frequency front-end circuits. Furthermore, nanometer RF-CMOS technology offers high quality factor of passive components, like transmission lines and inductors, have been provided by the thicker metal in the highest metallization layers. Besides nanometer CMOS technology offers great potential to achieve high performance, small chip area, low cost, low power dissipation, and long battery life-time for implementing analog and digital parts of baseband signal processing of potable devices.

The aggressive of scaling down of CMOS technology has prominent effects on supply voltage, where the maximum supply voltage is significantly reduced. Unlike the supply voltage, the threshold voltage of MOSFET devices \( V_T \) is reduced at a slower pace, as shown in Fig. 1.4. As results, the effective gate voltage \( V_{GS} - V_T \) becomes small. In digital circuits this increases the leakage current and delay time of the logic circuits. While, in analog circuit, the intrinsic gain of the MOSFET devices is reduced, due to fact that effective gate voltage is directly proportioned in MOSFET devices to transconductance \( gm \). Moreover, with low–voltage, the required linearity of the RF circuits is hard to achieve. Consequently, the performance of the entire RF front-end will degrade. This situation would become worse and worse as CMOS technologies continue to scale down.

### 1.2 Research Motivation

Motivated by the issues arise from the continually scaling of CMOS technology on RF circuits, the study on exploring new different circuit topologies and design techniques is presented in this thesis. The newly low-voltage fully integrated CMOS circuits, which can be adopted for high GHz regime (> 10 G\( Hz \)) RF front-end receivers, are designed, analyzed, and measured. Furthermore, a fully integrated 1-V current-mode front-end receiver with on chip LO signal generator and DC offset compensation circuit at 24-GHz RF application, is designed, analyzed, and measured by using the proposed circuits and techniques in this thesis.
1.3 Organization Of This Thesis

This thesis contains six chapters, which include analyses, designs, and implementations of CMOS low-noise amplifier (LNA), CMOS down-conversion mixer, and ISM RF front-end receiver.

Chapter 1 introduces the background, describes the research motivation, and explains the main topics of this thesis.

In Chapter 2, begins with brief introductory overviews of receiver architectures. The key building blocks of RF receiver front-end is also discussed. The performance of the CMOS high-frequency front-end circuits in the public domains is reviewed.

In Chapter 3, the technique of capacitive feedback matching has been presented to design an RFIC LNA, where the presented technique can be used with very low-voltages to achieve maximum power-gain and minimum NF simultaneously at any given amount of power dissipation. The full noise analysis of the LNA is supported by mathematical derivations and it is complemented and validated by measurements.

In Chapter 4, the design of low LO-power mm-wave RF CMOS quadrature balanced self-switching current-mode mixer has been presented. The presented mixer has high linearity with low-voltage supply, Besides, an area efficient 90-degree branch-line hybrid coupler is designed to deal with the issue on the combination of RF and LO signals at mm-waves frequencies.

In Chapter 5, 1-V current-mode front-end receiver with on chip LO signal generator and DC offset compensation circuit at 24-GHz RF application, is designed, and analyzed. The receiver composes of a transconductance low noise amplifier (TLNA), RF current-mode mixer, IF current-mode mixers, DC offset compensation, voltage control oscillator (VCO), and quadrature divided-by-two circuit(QD2). The TLNA proposed in presented in chapter 3 is used to amplified the RF input spectrum at 24 GHz with minimal noise contribution to enlarge the power difference between the received signal and noise, then the amplified RF input spectrum at 24 GHz is down-converted to an intermediate frequency (IF) of 8 GHz by using RF current-mode mixer presented in chapter 4, and a follow-up IF current-mode mixers are used in-phase I and quadrature Q paths to directly convert the
spectrum at IF frequency to zero frequency. The baseband signals are then applied to the DC offset compensation circuit to eliminate DC offset currents appear at the output of the IF current-mode mixer due to the self-mixing of the LO.

Finally, the main results and conclusions of this thesis are summarized in Chapter 6. Some suggestions and future works about the implementations of current-mode receiver.
Figure 1.1: Wireless communication landscape.
Figure 1.2: The unlicensed bandwidth available at 60 GHz.
Figure 1.3: The scenarios for short-range and long-range backbone wireless communication networks for home-RF applications.
Figure 1.4: The reduction of supply voltage and threshold voltage in accordance with the scaling of channel length of CMOS technologies.
Chapter 2

REVIEWS ON FRONT–END RECEIVERS, LOW–NOISE AMPLIFIERS, AND MIXERS

Because of the impossibility of digitizing RF spectrum at high GHz regime (> 10 GHz), the RF spectrum should be down-converted to a low frequency. Besides, all the unwanted RF signals adjacent to wanted RF spectrum have to be suppressed, so that they do not effect the operation of the down-converted devices. Moreover, in order to obtain the highest possible performance, the RF spectrum has to be amplified before it down-converted to minimize the noise contribution of the down-converted devices. All these tasks are what must be carried out by receiver.

From the above tasks the receiver should have an RF amplifier that can amplify the RF input spectrum with minimal noise contribution to enlarge the power difference between the received signals and noise. This amplifier is known as low-noise amplifier (LNA), and a down-converted device to change the center frequency of the RF spectrum, this device is known as mixer. In addition, to eliminating the interference of unwanted signal on the wanted RF, extra building blocks are required depending on the architecture of the receiver. In the following sections, it will be attempted to present the most important receivers architectures, Moreover, a brief overview of LNA and mixer circuits implemented in CMOS technology at high GHz regime will be described.
2.1 Receiver Architectures

2.1.1 Homodyne, Direct–Conversion, or Zero–IF Receiver

In a homodyne or direct-conversion receiver (DCR) which is depicted in Fig. 2.1 [14–21], the desired RF signal is directly down-converted to zero-IF in one-step frequency mixing with single LO signal. Therefore, in this type of the receiver, the LO frequency is equal to the RF frequency. The baseband signal is then filtered with a low-pass filter to select the desired channel.

For frequency- and phase-modulated signals, the down-conversion must provide quadrature outputs in order to avoid loss of signal information. The main advantage of DCR is that is does not possess the image problem when the incoming RF signal is directly down-converted to baseband without any IF stage. Another advantage is its simple architecture. However, the major disadvantage is DC offsets [22]. As shown in Fig. 2.2, the severe DC offsets can be generated at the output of the mixer when the leakage from the local oscillator is self-mixed with LO signal. The second source of DC offsets is the large nearby interferers leaking to the VCO and then self-mixing. This effect could saturate the following stage. The DC offsets can be removed by capacitive coupling. However, the signal power near DC will be lost. Hence, the size of capacitors should be chosen quite large. Feedback loops from the baseband or the digital part are also proposed to reduce the DC offsets. But these methods will increase the complexity of the direct-conversion receiver.

Equally critical is the flicker noise of the mixer since the mixer output is the baseband signal and can be easily corrupted by large noise. It is because that the flicker noise of active devices becomes the dominant noise source as the frequency below 1 MHz. The flicker noise should be considered in designing DCR. Active devices with large dimension can be chosen to reduce flicker noise. In addition, PMOS contributes less flicker noise than NMOS.

2.1.2 Heterodyne or IF Receivers

The most straightforward receiver architecture for implementing a cellular receiver front-end is evidently the heterodyne receiver, which is shown in Fig. 2.3 [23–28]. The
The main feature is the use of an Intermediate Frequency (IF). For this reason, the heterodyne is often also called the IF receiver.

The received RF signals from the antenna are first filtered by a band select filter, BPFRF1, which suppresses interferences residing outside of the application band. By removing these out-of-band blocking signals, which could saturate the following stages, the requirement of the dynamic range of the receiver can be relaxed considerably. A low noise amplifier (LNA) amplifies the received RF signals, which are then filtered by an image-reject filter, BPFRF2, to remove the image. The image has an offset of twice the intermediate frequency by the mixer. The received RF signals after BPFRF2 are down-converted to IF by the down-conversion mixer, and then passed through the channel-select filter BPFIF to remove the interferences at the adjacent channels. Finally, the channel-selected is demodulated into baseband I/Q signals to retrieve the desired signal information. The high-frequency noise and distortion from inter-modulation and high-order harmonics are removed by baseband low-pass filter LPFBB.

In the frequency translation, both the desired signal and image signal are mapped to the IF frequency after mixing. Although the image-reject filter BPFRF2 is used to attenuate the image signal, suitable attenuation of the image may not be practical unless the IF frequency is selected relatively high. The trade-off is that filtering at a high IF requires more complicated filters in order to maintain selectivity. It is difficult to realize an on-chip high-Q filter at the RF frequency. The required high-Q, high frequency image-reject filter is therefore placed off-chip. Consequently, the integration ability of the heterodyne or IF receiver is limited, and the cost is increased because of several off-chip filters are needed. Additional buffers to drive off-chip filters also require high power and reduce the gain of this kind of receivers.

The path mismatch is implied not a big issue because the image rejection does not rely on any matching between two signal paths, but is mainly done by the image-reject filter. Also LO feed-through and DC offset do not affect the signal quality since the desired signal frequency is never close to these frequencies. The same applies to self-mixing of either RF or LO signal. Another important property is that the channel selection occurs before the ADC. Hence, the ADC only requires handling minimum dynamic range. Due to the
bandpass nature of the channel, even the sub-sampling ADC can be used. Additionally, the number of bits can be kept low since both the out-of-band and in-band blocking signals have already been removed.

### 2.1.3 Image–Reject Receiver

The primary advantage of the image-reject receivers [29–33] is that they do not need image-reject filters. Without the image-reject filters, the IF frequency can be placed very low to reduce the design difficulty of the IF channel-select filter. Hartley [32] and Weaver [33] receivers are two famous image-reject receivers.

The architecture of Hartley receiver is shown in Fig. 2.4. The desired signal and the image signal are down-converted in both upper and lower paths. However, the desired signals at the points B and C are in-phase, while the image signals at the points B and C are out-of-phase. When the spectrum at the points B and C are combined, the image signals will be cancelled and the desired signals will be left.

The architecture of Weaver receiver is shown in Fig. 2.5. The Weaver receiver is different from the Hartley in that the quadrature mixers are used to replace 90-degree phase shifter in the signal path. The purpose of this replacement is to perform phase shifting not on the signal path, but on the second LO which is only a single sinusoidal tone. Therefore, the phase shifting accuracy can be well controlled.

The Image-Reject Ratio (IRR) of the Hartley and Weaver receivers is limited by the gain mismatches between I- and Q-path, the phase inaccuracy of quadrature LO signals, and the imperfect quadrature phase shifting. The IRR can be expected by

\[
IRR = \frac{1 + (1 + \varepsilon)^2 - 2(1 + \varepsilon) \cos(\theta)}{1 + (1 + \varepsilon)^2 + 2(1 + \varepsilon) \cos(\theta)}
\]

(2.1.1)

where \( \varepsilon \) and \( \theta \) are the gain and phase mismatch, respectively. For \( \varepsilon = 5\% \) and \( \theta = 5^\circ \), the IRR is 26 dB. Existing implementations of image rejection receivers typically achieve 30 ~ 40 dB for image rejection.
2.1.4 Wideband–IF Receiver

Shown in Fig. 2.6 [34, 35] is the architecture of wideband-IF receiver. The architecture of this receiver is similar to a combined technique of heterodyne receiver and Weaver image-reject receiver. In heterodyne receiver in Fig. 2.3, the channel selecting is performed using the RF local oscillator. However, the wideband-IF receiver uses a fixed RF local oscillator at the first mixing stage, and the entire received bands are translated to the fixed IF. In the second mixing stage, a tunable IF local oscillator is used to select the desired channel from the received entire bands, and the desired channel is translated to the baseband. Simultaneous image rejection is performed in the second mixing stage which uses quadrature frequency conversion.

Since the RF local oscillator is at fixed frequency, the phase noise performance of the oscillator can be optimized. Besides, it is relatively easier to design the IF VCO with a low phase noise. Nevertheless, the disadvantage is that the blocking signals at adjacent channels are translated to the baseband without filtering. Hence, the dynamic range or linearity shall be carefully considered. Take the linearity requirement into consideration, the gain of the receiver is mostly provided from the IF section. Leaving the gain to the IF section may increase the Noise Figure of the receiver. Besides, the image signal still interferes with the desired signal if I- and Q-path at the first stage have mismatches. Sometimes, an off-chip RF filter is required for high IRR.

2.1.5 Low–IF Receiver

The architecture of low-IF receiver is shown in Fig. 2.7 [36–38]. The low-IF receiver combines the advantage of heterodyne and direct-conversion receivers. The desired RF signals are down-converted to IF in one mixing step, which is similar to the direct-conversion receiver. Since the IF is higher than DC, DC offsets and flicker noise do not affect the desired signals. In low-IF receivers, poly-phase filters are used to remove the image; hence, the high-Q image-reject filter is not required. Because the polyphase filters are operated at the low intermediate frequency and are possible to be realized on-chip, low-IF receivers are obvious to have better integration capability than heterodyne receivers.
The IRR of the low-IF receiver is limited by the gain mismatches between I-path and Q-path, phase inaccuracy of the quadrature LO. The spectra flow of the low-IF receiver before and after down-conversion is shown in Fig. 2.8. The spectrum of complex signal (I+jQ) is represented. SIGpRF and IMpRF represent the spectrum of the desired signals and image signals. LOp represents the spectrum of the quadrature local oscillator. However, SIGnRF and IMnRF represent the crosstalk image signals of SIGpRF and IMpRF, respectively. LOn represents the crosstalk image signal of LOp. After the frequency conversion, the SIGpRF, SIGnRF, IMpRF, and IMnRF are down-converted to SIGnIF, SIGpIF, IMpIF, and IMnIF, respectively. As shown in Fig. 2.8, the image IMpIF mixes with the signal SIGpIF at the positive IF frequency $\omega_{IF}$, and hence cannot be removed following polyphase filter. Only the signals IMnIF and SIGnIF at the negative IF frequency $-\omega_{IF}$ can be removed by the following polyphase filter. Since mismatches in RF circuits are inevitable even in modern IC process, it is difficult to achieve high IRR without special and complicated techniques for low-IF receivers.

2.1.6 Double–Quadrature Receiver

Shown in Fig. 2.9 [39–41] is the architecture of Double-Quadrature Receiver (DQR) which is used to improve the IRR. The DQR shifts the phase of RF signal to quadrature and then the quadrature RF signals are downconverted to IF signals by mixing with quadrature LO signals. The DQR is less sensitivity to the imbalance of LO signals of I- and Q-path because the RF and LO signals are both put into quadrature phases. Since the RF signals are down-converted to IF, it is also immunity from the problem of DC offsets and flicker noises.

The spectra flow of the DQR before and after down-conversion is shown in Fig. 2.10. The spectrum of complex signal (I+jQ) is represented. SIGpRF and IMpRF represent the spectrum of the desired signals and image signals at the output of the quadrature generator. LOp, represents the spectrum of the quadrature local oscillator. However, SIGnRF and IMnRF represent the crosstalk image signals of SIGpRF and IMpRF, respectively. LOn represents the crosstalk image signal of LOp. After the frequency conversion, the SIGpRF, SIGnRF, IMpRF, and IMnRF are down-converted to SIGnIF, SIGpIF, IMpIF, and IMnIF, respectively. The same like the spectra of low-IF receiver in Fig. 2.8, the image
$IM_{pIF}$ mixes with the signal $SIG_{pIF}$ at the positive IF frequency $\omega_{IF}$, and hence cannot be removed following polyphase filter. Only the signals $IM_{nIF}$ and $SIG_{nIF}$ at the negative IF frequency $-\omega_{IF}$ can be removed by the following polyphase filter. However, the main difference between $DQR$ and low-IF receiver can be seen from the value of $IM_{pIF}$ of $DQR$ which can be represented as

$$IM_{pIF} = IM_{nRFLO_p}(ISR_{QG}ISR_{LO} + ISR_{mixers})$$  \hspace{1cm} (2.1.2)

where $ISR_{QG}$, $ISR_{LO}$, and $ISR_{mixers}$ denote the Image-to-Signal Ratio (ISR) of the quadrature generator, the local oscillator, and mixers, respectively. For $ISR_{QG}$, $ISR_{LO}$, and $ISR_{mixers} \ll 1$, the $ISR_{QG}ISR_{LO}$ term in (2.1.2) is negligible relative to $ISR_{mixers}$. Therefore, $IM_{pIF}$ is determined by the gain/phase errors of the mixers and $IM_{nRFLO_p}$.

The DQR exhibits better image-reject performance than the conventional low-IF receiver, because $IM_{pIF}$ is smaller and almost unaffected by $ISR_{LO}$. To achieve high IRR of the DQR, the symmetry of the layout in mixers between I/Q-paths should be regarded as reducing the amplitude of crosstalk image signals. Additionally, the polyphase filter must have a high capacity for rejecting images at the intermediate frequency.

The comparisons of the afore-mentioned receiver are listed in Table 2.1. The heterodyne receiver can achieve the best performance because it is immunity from the problem of I/Q-mismatches, DC offset and flicker noise. The expenses of the heterodyne receiver are high power consumption and poor integration ability. The DCR has the advantage of high integration ability and low-power consumption. However, the high performance is difficult to achieve because of the problems of DC offsets and flicker noise. Image-rejection, wideband-IF, and low-IF receivers achieve better performance than direct-conversion receiver, but the imbalance of LO signals will limit the IRR. Hence, off-chip high-Q RF filters are still required for high IRR. The DQR down-converts the RF signal to IF, so it will not be affected by DC offsets and flicker noise. Besides, the DQR is less sensitive to I/Q-imbalances, and off-chip high-Q RF filters are not required.
2.2 CMOS Low–Noise Amplifiers

The Low-Noise Amplifier (LNA) is one of the most important and critical parts in the receiver front-end. It is the first active circuit in the receiver part following the antenna as shown in Fig. 2.3. Due to its location in the receiver chain, it dominates the noise performance of the complete system.

In the design of RF-CMOS LNAs, it is known that the key performance parameters are power-gain and noise figure \((NF)\) besides the stability, linearity and isolation. The goal of LNA design is to achieve maximum power-gain and minimum \(NF\) simultaneously at any given amount of power dissipation. To reach this goal, the input impedance \((Z_{in})\) of a LNA must be kept close enough to the optimum source noise conjugate impedance \((Z_{n,opt})\). In order to illustrate the difficulties in achieving the above goal at frequencies above 10 GHZ, we study a number of CMOS LNAs circuit topologies.

Consider the common-source stage shown in Fig. 2.11(a) \([42–46]\). the \(Z_{in}\) and \(Z_{n,opt}\) of M1 are given as \([47]\):

\[
Z_{in} = \frac{1}{j\omega C_{gs}}
\]

\[
Z_{n,opt} = \frac{\omega(C_{gs} + C_{gd})}{\frac{\alpha^2 \delta}{5\gamma} (1 - |c|^2) + j \left(1 + \alpha|c| \sqrt{\frac{\delta}{5\gamma}} \right)}
\]

where \(\omega_o\) is the operating angular frequency, \(C_{gs}\) is the gate-source capacitance of MOSFET device, \(\gamma\) is the thermal noise coefficient, \(\delta\) is the gate induced current noise factor, \(c\) is the correlation coefficient theoretically equal to \(j0.395\) \([48]\), and \(\alpha \equiv gm/gd_0\) where \(gd_0\) is the zero-bias drain conductance.

By comparing (2.2.1) and (2.2.2), it can be seen that the optimum source impedance for input matching is inherently different from that of the noise matching in both real and imaginary parts. Thus, one cannot obtain both input matching and minimum \(NF\) simultaneously. For this reason \(NF\) of CS topology is generally high.
In Fig. 2.11(b), source degeneration inductor introduces a real part into the input impedance seen looking into the gate of M2. It is not hard to show that input impedance of M2 has the following form:

\[ Z_{in} = j\omega L_s + \frac{1}{j\omega C_{gs}} + g_m L_s \]  

(2.2.3)

While the \( Z_{n,opt} \) can be expressed as [49]:

\[ Z_{n,opt} = \frac{\sqrt{\alpha^2 \delta 5\gamma (1 - |c|^2) + j(1 + \alpha |c| \sqrt{\frac{\delta}{5\gamma}})}}{\omega (C_{gs} + C_{gd})(\alpha^2 \frac{\delta}{5\gamma} (1 - |c|^2) + (1 + \alpha |c| \sqrt{\frac{\delta}{5\gamma}})^2)} - j\omega L_s \]  

(2.2.4)

As can be seen from (2.2.3), the source degeneration generates the real part at the input impedance. This is important because there is no real part in \( Z_{in} \) without degeneration, while there is in \( Z_{n,opt} \). Therefore, if not excessive, \( L_s \) helps to reduce the discrepancy between the real parts of \( Z_{n,opt} \) and of \( Z_{in} \), the LNA [50–59]. Furthermore, from (2.2.3), the imaginary part of \( Z_{in} \) is changed by \( j\omega L_s \), and this is followed by the same change in \( Z_{n,opt} \), as shown in (2.2.4).

For stability reason [47], the drain of the input stage common-source should be connected to the low input impedance node. This inevitably decreases the power gain of the LNA, To retain the power-gain, multi-stage CS amplifiers topology is used in [44–46,50–56]. The 3-stage common-source amplifier used for K-band in [55,56] is shown in Fig. 2.12. In Fig. 2.12, source-degeneration inductor at first stage provides minimum noise figure with a real input impedance. In order to increase the stability of the LNA the source-degeneration inductor at following stages is used to provide low impedance. This topology is suitable for low-voltage application [44,51–53]. However it consumes large power.

Another method of providing stable CS amplifier is illustrated in Fig. 2.13 [42,43,57–59]. The common-gate amplifier is often used as cascade in the combination with the common-source amplifier, since the common-gate amplifier has low input impedance when it is driven from the current source, it can pass current through it to the load with near unity current gain. However, the difficulties in this topology are twofold. First, the pole at the
drain of M1 of the cascade LNA, as shown in Fig. 2.13, shunts a considerable portion of the RF current to ground, thereby lowering the gain and raising the noise contributed by M2. Second, with low-voltage, the cascade LNA has low linearity because of the required large voltage headroom.

Although common-gate (CG) amplifier can be design to exhibit an real input resistance for input power match at mm-wave [60], the minimum $NF$ and maximum power-gain cannot be achieved simultaneously. Due to the constrains of the input matching, the common-gate LNA has a lower bound of $NF$ equal to $1 + \gamma$ for perfect match, where $\gamma$ is the channel thermal noise coefficient.

A Common-gate with resistive feedback (CGRF) topology shown in Fig. 2.14 [61]. In This topology an external resistance $R_p$ is added to the traditional CG LNA in parallel with the input transistor to improve its noise performance. In order to implement $R_p$, shunt inductor $L_{shunt}$ is used, while $C_{shunt}$ is used to isolate the DC level of the source and drain. However, an extra area is required to implement $L_{shunt}$. Table 2.2 summarizes the performance parameters of the recent studies CMOS LNAs dating from 2001-2007.

### 2.3 CMOS Mixers

To recover the information carried by the RF spectrum at high frequencies, the down-conversion mixer converts the input RF spectrum at high frequencies to an intermediate frequency (IF) at the output through the use of a local oscillator signal (LO). Since the mixer locates immediately after the LNA in the receiver chain as shown in Fig. 2.3, it effects the linearity performance of the complete receiver [62]. A higher linearity allows a larger input power range from LNA. Linearity is the most difficult specification to achieve in designing a low-voltage mixer. Since the headroom is strictly limited in low-voltage mixer, high gain LNA may saturate mixer when a maximum signal or high-power blocking received. To handel the large signal from LNA, sufficient linearity is necessary. Besides the issue of the low-voltage of operation, RF design on advanced CMOS processes has been challenging on the high cost of the chip area, This translates to a need to reduce the design area for achieving a specific function under certain performance requirements [63].
The topology of the mixer at high-frequency, which have been reported in literature [61,63–72], can be classified into active and passive topologies depend on the DC power consummation. The passive mixers include differential pair mixer [61,68,71,72], cascade mixer [63], and the transconductance mixer [67]. While passive mixers include drain-pumped resistive mixer [64], gate-pumped resistive mixer [66], and resistive mixer [69,70].

In Fig. 2.15 [61], differential pair, which also known as Gilbert cell, consists of transconductance stage M1, differential switching pair M2 and M3, and load RL. The conversion gain of Gilbert cell mixer is proportional to RL, if the RL is large, its conversion gain would be large. With a large voltage drop, the Gilbert cell mixer is modified to the current-reuse bleeding mixer [71]. Bleeding mixer topology, as shown in Fig. 2.16, provides the better performance in terms of conversion gain, linearity, noise figure, and LO isolation. However, in order to drive differential pairs sufficiently to turn on and turn off, the LO signal strength should be large enough.

Cascade mixer is shown in Fig. 2.17 [63]. The mixer consists of two transistors M1 and M2 are connected in series. RF and LO signals are applied through M1 and M2 gates, respectively. The resultant output IF signal is extracted from the drain terminal of M2. A cascade type mixer has the advantage of providing good LO-RF isolation without the use of filter. Besides, the using of double-gate layout to implement M1 and M2, the capacitance at the drain of M1 can be minimized through a careful layout, which improves the conversion gain at mm-wave.

The simple schematic of transconductance mixer is shown in Fig. 2.18. In Fig. 2.18 the LO and RF signals are combined and applied to the gate of M1, to large the conversion-gain of M1, M1 is operated in the saturation region, with gate-source voltage \( V_{GS} \) of M1 is set close to its threshold Voltage \( V_{TH} \). However, due to the close operational frequencies of LO and RF signals, the RF-LO isolation is very poor. In order to improve the LO-RF isolation hybrid combiner is used in [67] as shown in Fig. 2.19, Although, the mixer in [67] required low input LO power, short-circuit drain nodes at LO frequency are required to improve stability. Thus, an open quarter-wave stub at the drain node is used. Besides, to provide DC biasing for M1 and M2 an extra area is required for implementing short quarter-wave stub. All this increase the chip size area.
The active mixer topologies can achieve low conversion loss or even gain, but the linearity of these active topologies is low, especially at moderate to low power consumption. Much higher linearity can be achieved with resistive mixers. Drain-pumped resistive mixer is shown in Fig. 2.20 [64]. In Fig. 2.20 LO and RF signals are applied to drain and gate of M1, respectively. The transconductance of M1 is a time variant function of drain-source voltage $V_{DS}$ and $V_{GS}$. At proper bias, the nonlinearities of the other elements are weak and can be neglected. The gate-pumped resistive mixer shown in Fig. 2.21 [66]. In gate-pumped resistive mixer LO and RF signals are applied to source and gate of M1. The transconductance of M1 is a time variant function of $V_{GS}$.

Another passive mixer topology is shown in Fig. 2.22 [69, 70], In this topology LO signal is applied to the gate of M1 via a matching network, a simple diplexer separates the RF and IF signals. The passive mixers have a significant advantage that RF and LO frequencies, which are close in the frequency value, are injected at different ports. Thus, the simplified filtered circuit would improve the LO-RF isolation. However, due to passive and resistive nature of the resistive mixers topologies, its have a relative high conversion loss. In addition they require high LO input power. Table 2.3 summarizes the performance parameters of the recent studies high-frequency CMOS mixers dating from 2004-2007.
Table 2.1: Comparison of receiver architecture.

<table>
<thead>
<tr>
<th></th>
<th>Heterodyne</th>
<th>Direct-Conversion</th>
<th>Image-Rejection</th>
<th>Wide-band IF</th>
<th>Low-IF</th>
<th>Double-Quadrature</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Performance</strong></td>
<td>Good</td>
<td>Poor</td>
<td>Moderate</td>
<td>Moderate</td>
<td>Moderate</td>
<td>Moderate</td>
</tr>
<tr>
<td><strong>DC-Offsets</strong></td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td><strong>1/f noise</strong></td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td><strong>Balance I/Q</strong></td>
<td>Not required</td>
<td>Accurate</td>
<td>Accurate</td>
<td>Accurate</td>
<td>Accurate</td>
<td>Moderate</td>
</tr>
<tr>
<td><strong>Image Rejection</strong></td>
<td>Good</td>
<td>Not required</td>
<td>Moderate</td>
<td>Moderate</td>
<td>Moderate</td>
<td>Good</td>
</tr>
<tr>
<td><strong>Integration Ability</strong></td>
<td>Poor</td>
<td>Good</td>
<td>Moderate</td>
<td>Moderate</td>
<td>Moderate</td>
<td>Good</td>
</tr>
<tr>
<td><strong>Power Dissipation</strong></td>
<td>High</td>
<td>Low</td>
<td>Low</td>
<td>High</td>
<td>Low</td>
<td>Low</td>
</tr>
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</table>
Table 2.2: Summary of recent CMOS LNA results.

<table>
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<td>[46]</td>
<td>4</td>
<td>10</td>
<td>-15/-17</td>
<td>-/-</td>
<td>45</td>
<td>2</td>
<td>20</td>
<td>0.18 μCMOS</td>
<td>Cascode 1 stage</td>
<td>2001</td>
</tr>
<tr>
<td>59</td>
<td>5.2</td>
<td>12</td>
<td>-12/-</td>
<td>-/-</td>
<td>47</td>
<td>-</td>
<td>17</td>
<td>0.18 μCMOS</td>
<td>Cascode 2 stages</td>
<td>2003</td>
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<tr>
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<td>6</td>
<td>10</td>
<td>-17/-</td>
<td>-/-</td>
<td>47</td>
<td>-</td>
<td>24</td>
<td>0.18 μCMOS</td>
<td>Cascode 2 stages</td>
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<td>-11.1/+2.04</td>
<td>54</td>
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<td>23.5</td>
<td>0.18 μCMOS</td>
<td>3 stages CS</td>
<td>2003</td>
</tr>
<tr>
<td>45</td>
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<td>5.8</td>
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<td>-4.8/+3</td>
<td>10</td>
<td>1.5</td>
<td>20</td>
<td>90 nm CMOS</td>
<td>1 stage CS</td>
<td>2003</td>
</tr>
<tr>
<td>55</td>
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<td>12.9</td>
<td>-11/-22</td>
<td>-11.1/+2</td>
<td>54</td>
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<td>23.7</td>
<td>0.18 μCMOS</td>
<td>3 stages CS</td>
<td>2004</td>
</tr>
<tr>
<td>55</td>
<td>6.9</td>
<td>8.9</td>
<td>-14/-12</td>
<td>-10.2/+2</td>
<td>54</td>
<td>1.8</td>
<td>25.7</td>
<td>0.18 μCMOS</td>
<td>3 stages CS</td>
<td>2004</td>
</tr>
<tr>
<td>61</td>
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<td>15</td>
<td>-/-</td>
<td>-/-</td>
<td>24</td>
<td>1.5</td>
<td>21.8</td>
<td>0.18 μCMOS</td>
<td>1 CG and 2 CS stages</td>
<td>2004</td>
</tr>
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<td>10.71</td>
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<td>-5/+5.16</td>
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<td>1.3</td>
<td>14</td>
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<td>2 stages CS</td>
<td>2005</td>
</tr>
<tr>
<td>53</td>
<td>3.9</td>
<td>13.1</td>
<td>-15/-20</td>
<td>-12.2/+0.54</td>
<td>14</td>
<td>1</td>
<td>24</td>
<td>0.18 μCMOS</td>
<td>2 stages CS</td>
<td>2005</td>
</tr>
<tr>
<td>52</td>
<td>5.5</td>
<td>9.2</td>
<td>-8/-4</td>
<td>-/+7</td>
<td>19</td>
<td>1</td>
<td>20</td>
<td>90 nm CMOS</td>
<td>2 stages CS</td>
<td>2005</td>
</tr>
<tr>
<td>51</td>
<td>3.2</td>
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<td>Cascode 2 stages</td>
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Table 2.3: Summary of recent high-frequency CMOS mixer results.

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<td>2007</td>
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* Voltage gain.
Figure 2.1: The block diagram of the homodyne, direct-conversion, or zero-IF receiver.
Figure 2.2: Two sources of DC offsets in the direct-conversion receiver.
Figure 2.3: The block diagram of the heterodyne or IF receiver.
Figure 2.4: The block diagram of the Hartley receiver.
Figure 2.5: The block diagram of the Weaver receiver.
Figure 2.6: The block diagram of the wideband-IF receiver.
Figure 2.7: The block diagram of the low-IF receiver.
Figure 2.8: Spectra flow of the low-IF receiver.
Figure 2.9: The block diagram of the double-quadrature receiver.
Figure 2.10: Spectra flow of the double-quadrature receiver.
Figure 2.11: a) The common-source amplifier as the input stage, b) The common-source amplifier with source degeneration inductor.
Figure 2.12: The schematic diagram of 3-stage common-source LNA.
Figure 2.13: The schematic diagram of cascode LNA.
Figure 2.14: The schematic diagram of Common-gate with resistive feedback (CGRF)LNA.
Figure 2.15: The schematic diagram of single-balanced mixer Gilbert cell mixer.
Figure 2.16: The schematic diagram of single-balanced mixer with current bleeding.
Figure 2.17: The schematic diagram of Cascade mixer.
Figure 2.18: The schematic diagram of transconductance mixer.
Figure 2.19: The schematic diagram of transconductance quadrature balanced mixer with hybrid combiner.
Figure 2.20: The schematic diagram of drain-pumped resistive mixer.
Figure 2.21: The schematic diagram of gate-pumped resistive mixer.
Figure 2.22: The schematic diagram of resistive mixer.
Chapter 3

CMOS LOW–NOISE AMPLIFIER UTILIZING THE TECHNIQUE OF CAPACITIVE FEEDBACK NETWORK

In this chapter, a CMOS low-noise amplifier (LNA) with a new input matching topology has been proposed, analyzed, and measured. The input matching network is designed through the technique of capacitive feedback matching network. The proposed LNA which is implemented in a 0.18 $\mu$m 1P6M CMOS technology is operated at the frequency of 12.8 GHz. It has a gain $S_{21}$ of 13.2 dB, a noise figure ($NF$) of 4.57 dB and an $NF_{\text{min}}$ of 4.46 dB. The reverse isolation $S_{12}$ of the LNA can achieve $-40$ dB and the input and output return losses are better than $-11$ dB. The input 1-dB compression point is $-11$ dBm and IIP3 is $-0.5$ dBm. This LNA drains 10 mA from the supply voltage of 1 V.

The proposed input matching method is discussed in Section 3.1 and its effect on the noise figure ($NF$) is presented in Section 3.2. The details of the designed CMOS circuit of the LNA are presented in Section 4.2. While in Section 3.4, it describes the experimental results. Finally, the summary is given in Section 4.4.
3.1 Proposed Input Matching Method

The input impedance of the LNA is designed to match with the antenna, in order to prevent the incoming signal from reflecting back and forth between the LNA and the antenna. Generally, the antenna has 50-Ω load to the LNA. Unfortunately, the input impedance of a MOSFET device is inherently capacitive, so the matching with 50-Ω resistive input impedance is not an easy task. Thus, a capacitive feedback matching technique is proposed to overcome this problem [75].

The common-source amplifier as the input stage is shown in Fig. 3.1, where $Z_s$ is the impedance seen from the right node of the input matching inductor $L_g$, $Z_{in}$ is the input impedance of M1, $C_{gd}$ is the gate-drain capacitance, $C_{gs}$ is the gate-source capacitance, $C_{out}$ is the output loading capacitance which is the input capacitance of the next stage, $R_s$ is the signal-source resistance, and $V_s$ is the input signal voltage source. By using Millers theorem on $C_{gd}$, the input impedance $Z_{in}$ can be derived as

$$Z_{in} = \frac{R_f}{Q_f^2 + 1} + \frac{1}{j\omega_o(C_{gs} + C_{gd})(\frac{1}{Q_f^2} + 1)}$$ (3.1.1)

where

$$Q_f = \frac{\omega_o(C_{gs} + C_{gd})R_f}{g_m C_{gd}}$$ (3.1.2)
$$R_f = \frac{1}{g_m C_{out}}$$ (3.1.3)

$g_m$ is the transconductance of M1, and $\omega_o$ is the operating angular frequency. As it can be seen from the above equations, both $C_{gd}$ and $C_{out}$ with $g_m$ together providing a real term $R_f$ which contributes to the real input impedance in $Z_{in}$. They are called the capacitive feedback matching network.

3.2 The Noise Analysis of the Proposed Input Matching Method

In the LNA design, input power match is essential but not sufficient. It is also vital for a LNA to satisfy the noise performance requirement, so that the circuit itself does not
degrade the output signal-to-noise ratio (SNR) to an unacceptable level. Thus, a careful noise analysis on the capacitive feedback matching technique is developed to establish the principle of operation clearly and find the limits on noise performance. A brief review of the standard CMOS noise sources will facilitate the analysis.

3.2.1 Noise Sources

Fig. 3.2 shows the small-signal model of the equivalent circuit for the noise analysis. Three noise sources have been considered in Fig. 3.2. They are the thermal noise of the source resistance $i_{n,R}$, the thermal noise of the channel current $i_{n,d}$, and the gate induced current noise $i_{n,g}$. They can be expressed as [48]

$$\overline{i_{n,R}} = 4kT \frac{1}{R_s} \Delta f$$  \hspace{1cm} (3.2.1)$$

$$\overline{i_{n,d}} = 4kT \gamma g_{d0} \Delta f$$  \hspace{1cm} (3.2.2)$$

$$\overline{i_{n,g}} = 4kT \delta \frac{\omega^2 C_g^2}{5g_{d0}} \Delta f$$  \hspace{1cm} (3.2.3)$$

where $k$ is the Boltzmann’s constant, $T$ is the absolute temperature, $R_s$ is the source resistance, $g_{d0}$ is the zero-bias drain conductance, $\gamma$ is the thermal noise coefficient, $\Delta f$ is the noise bandwidth in hertz, and $\delta$ is the gate induced current noise factor.

According to [48], there is a correlation between the gate induced current noise $i_{n,g}$ and the thermal noise of the channel current $i_{n,d}$. This correlation can be treated by separating $i_{n,g}$ into two parts. $i_{n,gc}$ is the part that fully correlated with thermal noise of the channel current $i_{n,d}$, whereas $i_{n,gu}$ is the uncorrelated part. Hence, the gate induced current noise can be written as

$$\overline{i_{n,g}} = 4kT \delta \frac{\omega^2 C_g^2}{5g_{d0}} (1 - |c|^2) \Delta f + 4kT \delta \frac{\omega^2 C_g^2}{5g_{d0}} |c|^2 \Delta f,$$

\hspace{1cm} (3.2.4)

where the correlation coefficient $c$ is defined as [48]

$$jc = \frac{i_{n,g} i_{n,d}^*}{\sqrt{\overline{i_{n,g}^2} \overline{i_{n,d}^2}}},$$

\hspace{1cm} (3.2.5)
Because of the correlation, special attention must be paid to the reference polarity of the correlated component. The value of $c$ is positive for the polarity shown in Fig. 3.2.

### 3.2.2 Capacitive Feedback Matching Network Noise Analysis

Noise performance is usually evaluated with noise figure ($NF$) which indicates the noise suppression ability of the circuit. Noise figure is defined as

$$ NF = 10 \log(F), \quad (3.2.6) $$

where $F$ is the noise factor which is defined as the total output noise power divided by the noise power at the output due to the input source. $F$ can be expressed as

$$ F = \frac{i_{n,o,tot}^2}{i_{n,o,Rs}^2} = \frac{i_{n,o,Rs}^2 + i_{n,o,g+d}^2}{i_{n,o,Rs}^2}, \quad (3.2.7) $$

where $i_{n,o,tot}^2$ is the mean-squared of the total output noise current, $i_{n,o,Rs}^2$ is the mean-squared output noise current due to $i_{n,Rs}$, and $i_{n,o,g+d}^2$ is the mean-squared output noise current due to $i_{n,d}$ and $i_{n,g}$. Considering correlation, $i_{n,o,g+d}^2$ can be re-expressed as

$$ i_{n,o,g+d}^2 = (i_{n,o,d}^* + i_{n,o,g}^*)(i_{n,o,d} + i_{n,o,g}) = i_{n,o,d}^2 + 2Re(i_{n,o,d}i_{n,o,g}^*) + i_{n,o,g}^2. \quad (3.2.8) $$

From (3.2.5), (3.2.7), and (3.2.8), Noise factor can be expressed as

$$ F = \frac{A^2 i_{n,d}^2 + 2Re(AB^*c\sqrt{i_{n,g}^* i_{n,d}^*}) + B^2 i_{n,g}^2}{D^2 i_{n,Rs}^2}, \quad (3.2.9) $$

50
where

\[ A = \frac{i_{n,o,d}}{i_{n,d}} = 1 \]  
(3.2.10)

\[ B = \frac{i_{n,o,g}}{i_{n,g}} = \frac{R_S + SL_g}{R_s + SL_g + Z_{in}} Z_{in} g_m \]  
(3.2.11)

\[ D = \frac{i_{n,o,Rs}}{i_{n,Rs}} = \frac{R_S}{R_s + SL_g + Z_{in}} Z_{in} g_m. \]  
(3.2.12)

Finally, the noise factor for a capacitive feedback matching network is obtained from (3.2.9)-(3.2.10) as

\[
F = 1 + \frac{\gamma}{\alpha g_m R_s} \left\{ \left| c \right| \alpha \sqrt{\frac{\delta}{5\gamma}} \right\}^2 
+ \left( R_s^2 - s^2 L_g^2 \right) \left( \frac{1}{R_f} - \frac{\alpha^2 \delta}{5\gamma} \left( 1 - \left| c \right|^2 \right) s^2 C_i \right) 
- \left( s C_i R_s \right)^2 \left[ 1 + \left| c \right| \alpha \sqrt{\frac{\delta}{5\gamma}} \right] + \frac{2 R_s}{R_f} \right\}, \]  
(3.2.13)

where \( C_i = C_{gs} + C_{gd} \) and \( \alpha \equiv g_m / g_{d0} \). By taking the derivatives of (3.2.13) with respect to \( R_s \) and \( L_g \) and let the derivatives equal to zero, optimum source noise impedance, \( Z_{n,opt} = R_{n,opt} + j\omega L_{n,opt} \), corresponding to minimum noise figure can be written as

\[
Z_{n,opt} = \sqrt{\frac{\alpha^2 \delta}{5\gamma} \left( 1 - \left| c \right|^2 \right) + \frac{1}{Q_f^2} + j \left( 1 + \alpha \left| c \right| \sqrt{\frac{\delta}{5\gamma}} \right)} 
\left\{ \frac{\alpha^2 \delta}{5\gamma} \left( 1 - \left| c \right|^2 \right) + \frac{1}{Q_f^2} + \left( 1 + \alpha \left| c \right| \sqrt{\frac{\delta}{5\gamma}} \right)^2 \right\} 
\times \frac{1}{\omega \left( C_{gs} + C_{gd} \right)}. \]  
(3.2.14)

Using (5.1.1), (3.2.14) can be re-expressed in \( Z_{n,opt}^* \) as

\[
Z_{n,opt}^* = \text{Re}[Z_{n,opt}] + \eta \text{Imag}[Z_{in}]. \]  
(3.2.15)
\[ \eta = \frac{\left(1 + \frac{1}{Q_f^2}\right) \left(1 + \alpha |c| \sqrt{\frac{\alpha}{5\gamma}}\right)}{\left\{\alpha^2 \delta \left(1 - |c|^2\right) + \frac{1}{Q_f^2} + \left(1 + \alpha |c| \sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}}. \] (3.2.16)

From (3.2.15), the imaginary part of \( Z_{\text{n,opt}}^* \) is nearly the same as the imaginary part of \( Z_{\text{in}} \) and expressed as \( \eta \text{Imag}[Z_{\text{in}}] \).

For the circuit in Fig. 3.1, the condition for maximum input power transfer (thus power-gain) is \( Z_{\text{in}} = Z_s^* \) and that for the minimum noise figure is \( Z_s = Z_{\text{n,opt}} \). Ideally, we have the condition for maximum power-gain and minimum noise figure is \( Z_{\text{in}} = Z_{\text{n,opt}}^* \). From (5.1.1), (3.2.14), and (3.2.15), this condition can be satisfied if \( \eta \) is close to 1 and

\[ \frac{1}{g_m(Q_f^2 + 1)} \frac{C_{\text{out}}}{C_{\text{gd}}} = R_{s_{\text{n,opt}}}. \] (3.2.17)

In the proposed technique of capacitive feedback matching network, the value of \( \eta \) is more close to 1 when compared to the inductive source-degeneration technique. Moreover, (3.2.17) can be satisfied by designing suitable device parameters \( g_m, C_{\text{gd}}, \) and \( C_{\text{gs}} \) of the device M1 as shown in Fig. 3.3, which are related to gate-source voltage \( V_{gs} \) and transistor size \( W/L \). In other words, the proposed design technique and input stage in Fig. 3.1 help to maximize the power-gain and to minimize the noise figure simultaneously by bringing \( Z_{\text{in}} \) close to the optimum source noise conjugate impedance \( Z_{\text{n,opt}}^* \).

It can be seen from (5.1.1) that without the feedback gate-drain capacitance \( C_{\text{gd}} \), the input impedance of the common-source amplifier would have no real part. However, the optimum source noise impedance \( Z_{\text{n,opt}} \) in (3.2.14) has a real part. Then it is impossible to satisfy the condition \( Z_{\text{in}} = Z_{\text{n,opt}}^* \). In the proposed technique, \( C_{\text{gd}} \) and the capacitive feedback matching network are used to satisfy the condition. Thus the technique is called the technique of capacitive feedback matching network.
3.3 Circuit Implementations

The complete circuit of the proposed LNA with the output stage is shown in Fig. 3.4 where in the LNA stage, M1 with the input amplifier transistor and M2/M3 form the current-mirror amplifier as the second amplifier stage. The effective transconductance of the two stages is given by

\[ |G_{eff}| = \frac{1}{2R_s} \left( \frac{\omega_T}{\omega_o} \right) \frac{g_{m3}}{\omega_o C_{out}} = \frac{1}{2R_s} \left( \frac{\omega_T}{\omega_o} \right)^2 \xi, \]

(3.3.1)

where \( \omega_T \) is unit gain angular frequency, \( g_{m3} \) is the transconductance of M3, \( C_{out} \) is the total capacitance at the drain of M1 which is dominated by \( C_{gs} \) of M3, and \( \xi \) is a constant approximately equal to 1 under the condition of \( C_{out} \) approaching \( C_{gs} \) of M3. So using coupling capacitor between M1 and M3 to isolate the bias levels results in serious degradation on the gain due to the parasitic capacitance of the bottom-plate of coupling capacitor. For this reason, M2 is used as the master transistor of the MOSFET current-mirror amplifier along with the slave transistor M3. The size of M2 is chosen to be very small as compared to M1 and M3 to obtain a higher current gain. Moreover, from Hspice noise simulation results, M2 contributes less than 1.5% of overall LNA noise figure. Since the cascode structure is not adopted, the proposed LNA can be operated at a low supply voltage.

In order to make the parallel resonance circuit behave like a capacitive load, a parallel resonance circuit composed of L2 and the parasitic capacitance at the drain of M1 resonates at the frequency below the operating frequency of the LNA. R1 is used to ensure stability. C1 and C2 are dc blocking capacitors. The tank L3 and C3 is used to resonate with the parasitic capacitances of the gate M4. R2 is used to provide the gate dc bias of M1 and chosen large enough that its equivalent noise current is small enough to be ignored.

In the output stage, the output buffer composed of M4, L4, C4, and R3, is designed for the measurement purpose. R3 is used to provide the gate dc bias of M4, C2 and C4 is the dc blocking capacitor. The output inductor L4 is used to resonate with the parasitic capacitances at the drain of M4. The voltage gain of the buffer is unity.

Form (3.2.16) and under the condition of the short channel devices, the expected noise parameters of device are \( \alpha = 0.6, \delta/\gamma = 2, |c| = 0.5 \) and \( Q_f = 2 \). In the proposed LNA, the \( \eta \) is 0.87, while the \( \eta \) of the LNA with source degenerative method is equal to 0.82.
It is important to notice that some amount of mismatch in the input matching $Z_{in} = Z_s^*$ has negligible effect on the LNA performance, while the mismatch in $Z_s = Z_{n,opt}$ directly affects the $NF$ [49]. Thus $Re[Z_{in}]$ is designed to be equal to the calculated $R_{sn,opt}$.

### 3.4 Experimental Results

Based upon the proposed technique of capacitive feedback matching network and LNA structure, an experimental chip of a LNA operated at 13 GHz was designed and fabricated in a 0.18 $\mu$m 1P6M CMOS technology. The chip photograph is shown in Fig. 6.1 and the total die area is 746.5$\mu$m $\times$ 884.6$\mu$m including all testing pads and dummy metals. The performance of the fabricated LNA circuit was tested through on-wafer probing technique. The measured and simulated S21 and input return loss S11 are shown in Fig. 3.5. In Fig. 3.5 the measured S21 is 13.2 dB at 12.8 GHz. The measured and simulated output return loss S22 and reverse isolation S12 are shown in Fig. 3.6. As can be seen from Figs. 3.5 and 3.6, the measured reverse isolation S12 of the LNA achieves $-40$ dB whereas the input and output return losses are better than $-11$ dB. The stability K-factor and B-factor is shown in Fig. 3.7. Since stability K-factor and B-factor are larger than 1 and 0, respectively, the proposed LNA is unconditional stable. The frequency shift from 13 GHz to 12.8 GHz is mainly due to the inaccurate modeling of planar inductor at high-frequency. Besides, the parasitic capacitances that results from metal-fill, RF-pads, and interconnection lines have minor contribution to the shift.

The fabricated LNA has a $NF$ of 4.57 dB and the minimum noise figure $NF_{min}$ of 4.46 dB at 12.8 GHz as shown in Fig. 3.8. As may be seen from Fig. 3.8, $NF$ and $NF_{min}$ are very close to each other over a large frequency range. Thus the proposed LNA is insensitive for operating frequency variations. The measured output power versus the input power is shown in Fig. 3.9 where the input referred 1-dB compression gain is $-11$ dBm. The measured two-tone test results are shown in Fig. 3.10. In Fig. 3.10 the measured IIP3 is $-0.5$ dBm.

The measured performance parameters are summarized in Table 3.1 where comparisons with other published works are also listed. In order to compare the performance of our LNA design, three different figures of merit $FOMs$ previously presented in literature have
been considered herein. In detail, $FOM_1$ is defined as the ratio between the power-gain ($S_{21}$) in $dB$ and the power consumption in Watt. $FOM_2$ is defined to include the $NF$ of the LNA. $FOM_3$ takes into account the IIP3 and the operating frequency $f_c$ as well. They can be written as [76]

$$FOM_1 = \frac{S_{21}}{P_{DC} \times 10^{-3}}$$

(3.4.1)

$$FOM_2 = \frac{10^{S_{21}/10}}{[10^{NF/10} - 1] \times P_{DC} \times 10^{-3}}$$

(3.4.2)

$$FOM_3 = \frac{[10^{(S_{21}+IIP3)/10}] \times \frac{f_c}{10^9}}{[10^{NF/10} - 1] \times P_{DC} \times 10^{-3}}$$

(3.4.3)

Based upon Table 3.1, it is clear that the proposed LNA outperforms all the other LNAs with a higher value of FOM. As expected, the proposed LNA with the technique of capacitive feedback matching network has high power-gain and low-noise figure under low power dissipation. It can be operated at a low supply voltage of 1 V since the cascode structure is not adopted. However, it still has a high reverse isolation.

### 3.5 Summary

A new LNA structure with the technique of capacitive feedback matching network is proposed and analyzed. An experimental chip of 13-GHz LNA has been successfully designed and fabricated. The measurement results have shown that the proposed LNA can achieve minimum noise figure and maximum power-gain simultaneously. In additions, the $NF$ is insensitive to the large operating frequency shift.
Table 3.1: The measured performance parameters of the fabricated LNA and comparisons with other published LNAs.

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<thead>
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<th></th>
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<td>0.18µm</td>
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<td>0.18µm</td>
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<td>CMOS</td>
<td>CMOS</td>
<td>CMOS</td>
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<tr>
<td><strong>Freq. (GHz)</strong></td>
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<td>14</td>
<td>8</td>
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<tr>
<td><strong>Gain (dB)</strong></td>
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<td>10.71</td>
<td>13.5</td>
<td>12.2</td>
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<tr>
<td><strong>NF (dB)</strong></td>
<td>4.57</td>
<td>3.16</td>
<td>3.2</td>
<td>3.7</td>
<td>6.4</td>
</tr>
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<td><strong>IIP3 (dBm)</strong></td>
<td>−0.5</td>
<td>1.6</td>
<td>−3.2*</td>
<td>−1.3*</td>
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<tr>
<td><strong>Power (mW)</strong></td>
<td>10</td>
<td>28.6</td>
<td>22.4</td>
<td>19.6</td>
<td>10</td>
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<tr>
<td><strong>Supply (V)</strong></td>
<td>1</td>
<td>1.3</td>
<td>1</td>
<td>1</td>
<td>1.5</td>
</tr>
<tr>
<td><strong>S11 (dB)</strong></td>
<td>−11</td>
<td>−10</td>
<td>−5.8</td>
<td>−5.4</td>
<td>−</td>
</tr>
<tr>
<td><strong>Chip Size (mm²)</strong></td>
<td>0.746 × .885</td>
<td>.88 × .77</td>
<td>–</td>
<td>1 × .9</td>
<td>.7 × .8</td>
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<td><strong>FOM1</strong></td>
<td>1.32</td>
<td>0.374</td>
<td>0.6</td>
<td>0.622</td>
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<tr>
<td><strong>FOM2</strong></td>
<td>1.12</td>
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<td>0.92</td>
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<td><strong>FOM3</strong></td>
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<td>7.2</td>
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<td>7.4</td>
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</table>

*The IIP3 is predicted by input P1dB+10dBm
Figure 3.1: The common-source amplifier as the input stage.
Figure 3.2: The small-signal equivalent circuit for noise calculations.
Figure 3.3: The design steps for capacitive feedback matching network LNA.
Figure 3.4: The complete circuit diagram of proposed LNA.
Figure 3.5: The measured and simulated $S_{11}$ and $S_{21}$ results of the proposed LNA.
Figure 3.6: The measured and simulated $S_{22}$ and $S_{12}$ results of the proposed LNA.
Figure 3.7: The measured stability K-factor and B-factor of the proposed LNA.
Figure 3.8: The measured and simulated noise figure $NF$ and minimum noise figure $NF_{min}$ of the proposed LNA.
Figure 3.9: The LNA measurement results of $P_{in}$ versus $P_{out}$. 
Figure 3.10: The LNA measurement results of two-tone test.
Figure 3.11: The chip photograph of the proposed LNA utilizing the technique of capacitive feedback network.
Chapter 4

CMOS SELF–SWITCHING CURRENT–MODE MIXER

This chapter describes the analysis and measurement of a CMOS quadrature balanced current-mode mixer with 90° branch-line hybrid coupler and self-switching current-mode devices. The proposed mixer, using 0.13-μm 1P8M CMOS technology, can down-convert 60–GHz RF signal to 2–GHz intermediate frequency (IF) signal, with a LO power of 0 dBm at 58 GHz. In the design, the mixer had a single-end conversion gain of 1 dB and an input-referred 1dB compression point of 2 dBm. The LO-RF isolation of the mixer can achieve –37 dB while using 3 mA from a supply voltage of 1.2 V.

In this chapter, both the operational principle and circuit implementation are presented in Section 4.1 and 4.2, while the experimental results themselves are described in Section 5.2. Finally, the summary is given in Section 4.4.

4.1 Operational Principle Of Self–Switching Current–mode Mixer

The concept of self-switching current-mode circuit is shown in Fig. 4.1 where Ma is an nMOS device. In Fig. 4.1, both the RF signal current $i_{\text{rf}}$ and the LO signal current $i_{\text{lo}}$ are applied to the source together through a combiner, usually a filter or directional coupler. $I_{TH}$ is a DC current added with $i_{\text{rf}}$ to control the conversion gain. The resonator at the output port (capacitor $C_T$ and inductor $L_T$) is used as bandpass filter to reject all signals except IF. When $i_{\text{lo}} + I_{TH}$ is high enough in the direction of the source current $i_s$, Ma is
switched on, and remains on only as long as this condition lasts, after which it is switched off. This property is adopted to form the down-conversion mixer.

Assuming that the local oscillator current $i_{lo}$ is much larger than the input signal current $i_{rf}$, the ac current gain $A_i = i_d/i_{rf}$ of Ma can be considered as a function of the sinusoidal LO current only, as shown in Fig. 4.2. $A_i$ can, therefore, be considered as periodically varying at the LO frequency and represented by a Fourier series as

$$A_i = \alpha_0 + \alpha_1 \sin \omega_{LO}t + \alpha_2 \sin 2\omega_{LO}t + \ldots + \alpha_j \sin j\omega_{LO}t + \ldots + \alpha_n \sin n\omega_{LO}t$$  \hspace{1cm} (4.1.1)

$$\alpha_j = \frac{1}{\pi} \int_{0}^{2\pi} A_i \sin(j\omega_{LO}t) d(\omega_{LO}t)$$  \hspace{1cm} (4.1.2)

where $\omega_{LO}$ is the radian frequency of LO signal, and $\alpha_0, \alpha_1, \ldots, \alpha_j, \ldots, \alpha_n$ are Fourier coefficients. When a small RF current signal $i_{rf} = I_{RF} \cos \omega_{RF}t$ is applied to the source of M1, the alternating drain current $i_d = A_i i_{rf}$ can be written as

$$i_d = \alpha_0 I_{RF} \cos \omega_{RF}t + \frac{1}{2} I_{RF} \sum_{j=1}^{n} \alpha_j \sin(\omega_{RF} + j\omega_{LO})t + \frac{1}{2} I_{RF} \sum_{j=1}^{n} \alpha_j \sin(\omega_{RF} - j\omega_{LO})t$$  \hspace{1cm} (4.1.3)

where $\omega_{RF}$ is the radian frequency of RF signal, and $I_{RF}$ is the RF signal amplitude. From (4.1.3), the $j^{th}$ harmonic conversion current gain $A_{cj}$ at the $j^{th}$ harmonic of the LO is $\frac{\alpha_j}{2}$. By substituting the value of the Fourier coefficient $\alpha_j$ in (4.1.2), can be rewritten as

$$A_{cj} = \frac{\alpha_j}{2} = \frac{1}{2\pi} \int_{0}^{2\pi} A_i \sin(j\omega_{LO}t) d(\omega_{LO}t)$$  \hspace{1cm} (4.1.4)

For the special case $n = 1$, the fundamental down-conversion current gain is $A_{c1}$ and $\omega_{IF}$ is equal to $\omega_{RF} - \omega_{LO}$. Fourier analysis is applied to $A_i$, where a sinusoidal waveform of $i_{lo}$ with 4m+1-points from -2m to 0 and from 0 to 2m. As derived in the Appendix, $A_{c1}$ can be expressed as

$$A_{c1} = \frac{1}{4m} \left[ (C_m - C_{-m}) + 2 \sum_{P=1}^{m-1} (C_P - C_{-P}) \sin(P \frac{\pi}{2m}) \right]$$  \hspace{1cm} (4.1.5)

As may be seen from (4.1.5), and since $C_{-2m}, \ldots, C_0, \ldots, C_{2m}$ are positive terms, it
can be found that to achieve a higher conversion gain, $C_{-2m}$ to $C_{-1}$ should be set to 0. Therefore, $A_{c1} = 0$ in approximate one half of a LO period. In addition, $C_1$ to $C_{2m}$ should be maximized this can be done through controlling $I_{TH}$ as shown in Fig. 4.2.

### 4.2 Circuit Implementations

The schematic diagram of the proposed 60-GHz CMOS down-conversion quadrature balanced mixer is shown in Fig. 4.3. In Fig. 4.3, Ma5 and Ma6 are the self-switching devices, each biased by $\frac{1}{2}I_{TH}$. $I_{TH}$ is controlled by $I_1$ and $I_2$ ($I_{TH} = I_2 - I_1$) through diode-connected transistors M3 and M2, respectively. The two parallel LC resonant tanks (L1, C2) and (L2, C3) at the output ports are used to select the IF frequency at 2 GHz. The 90° branch-line hybrid coupler, which consists of transmission-lines T3-T6, each with the characteristic impedance of 60 Ω at 60 GHz, are used to provide a 90° phase delay and achieve isolation between the LO and RF ports. The common-gate amplifier, consisting of M1, transmission-lines T1 and T2 with a total length equal to 300 μm, and bypass capacitors C4 and C5, is used to match with the RF input port impedance of 50 Ω. C1 is the DC blocking capacitor to isolate the LO port from DC source. Moreover, the two output source-follower buffers M7 and M8 are designed for measurement purposes to drive the 50 Ω input port of the network analyzer.

The proposed mixer offers two advantages. First, it has a self-switching device at its triode region with low operating power and high linearity. Second, the gate node is connected to VDD, an AC ground, and the drain node is short-circuited at LO frequency, which reduces the required LO power [78] and improves the stability at LO frequency [70]. And because the design of the proposed mixer must deal with the issue on the combination of LO and RF signals, a 90° branch-line hybrid coupler [78] and the quadrature balanced mixer architecture are designed in.

At high operating frequencies, the hybrid can be easily integrated onto a chip, but it suffers from a large insertion loss due to the high substrate loss of the standard CMOS. In order to reduce the effect of the substrate loss, the branch-line and through-line lengths of the hybrid are reduced from $\lambda/4$ to $\lambda/6.4$ and $\lambda/10$, respectively, based on the methodology [79] of a short high-impedance transmission line with shunt lumped capacitors.
In the methodology proposed in [79], the maximum transmission line length reduction depends on the maximum characteristic impedance of the transmission line. Conventionally, both microstrip-line (MSL) and coplanar waveguide (CPW) are used to implement the transmission line. However, the maximum characteristic impedance of MSL depends on the distance between the top-layer and bottom-layer metals, which is fixed for a given CMOS technology. In the CPW transmission line shown in Fig. 4.3, the signal-to-ground spacing $W$ can be used to increase the impedance of CPW, while the signal width $d$ controls the conductor loss. Additionally, the underpass metal, which connects the two planar grounds to suppress unwanted odd CPW mode, is used with intrinsic device capacitances to implement the required shunt capacitors. Moreover, CPW is more area efficient than MSL. In MSL the isolation between the adjacent lines must be considered because the coupling between two adjacent lines changes the characteristic impedance. Consequently, an extra separation distance between the adjacent elements should be considered to eliminate the unwanted coupling effects. This drawback can be avoided in CPW by surrounding the signal line with two adjacent well-grounded lines. For these reasons, the CPW is used to design the $90^\circ$ branch-line hybrid.

4.3 Experimental Results

The proposed mixer operated at $60\,GHz$ was designed and fabricated in $0.13\,\mu m\,1P8M\,CMOS$ technology. The chip photograph is shown in Fig. 4.5, and the total die area is $1400\,\mu m \times 1040\,\mu m$ including all test pads and dummy metals. The performance of the fabricated mixer circuit was tested through an on-wafer probing technique.

The test setup is shown in Fig. 4.6, where a signal generator with an external source module are used as $58\,GHz$ LO source followed by $10\,dB$ directional coupler. A power sensor followed by a power meter is connected to the coupler’s coupled port to monitor the LO power levels of the through port. The coupler’s through port is connected through the waveguide connector of $100\,\mu m$ V-band microwave probe to the DUT.

The $60\,-\,GHz$ RF signal is generated by the signal generator and followed by a source module. However, because this source module output power level is fixed and not adjustable, a variable attenuator is added to the RF port while the rest of test setup is
identical to the LO port. The output IF signal is measured using differential 150 μm probes through the bias-Tee, where one IF port is connected to 50 Ω for termination, while the other IF port is connected to a spectrum analyzer. The loss of probes, bias-Tees, coaxial cables, and the waveguide connecters were measured separately and used to correct the measured results. The measured results are accurate to within ±1 dB.

The measured and simulated output IF power versus the input RF power at 0 dBm LO power is shown in Fig. 4.7, where the input referred to as 1dB compression again is up to 2 dBm. The measured and simulated conversion gain values versus the LO power at 58 GHz with RF signal at 60 GHz are shown in Fig. 4.7, which shows that the single-ended conversion gain is 1 dB at 0 dBm LO power. The discrepancy of 2 dB between measurement and simulation is likely due to the accuracies of the measurement system (±1 dB), and the modeling of MOS transistor at high frequencies. The measured LO-RF isolation is better than −37 dB, as shown in Fig. 4.9. Besides, the measured 3 dB RF and IF bandwidth of the mixer are 6.3 GHz and 400 MHz, respectively. The fabricated mixer drains 3mA from a power supply of 1.2 V.

Finally, the measured performance of the fabricated mixer is summarized in Table 4.1, where comparisons with other published 60-GHz mixers are also provided. From Table 4.1, the proposed current-mode mixer can achieve high linearity and a higher conversion gain with low LO power, while at the same time achieving a smaller chip area by reducing the transmission lines used in the proposed mixer.

4.4 Summary

This chapter has proposed the fabrication and analysis of a CMOS quadrature balanced current-mode mixer based on a self-switching device. An area-efficient on-chip 90° branch-line hybrid coupler is designed to combine the LO and RF signals with an isolation better than −37 dB. The measurement results have shown that the proposed current-mode mixer is suitable for the applications of low-voltage and lower-power RF communication systems.
Table 4.1: The performance summaries of the proposed mixer and comparisons with other published mixers.

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<td>RF Freq.</td>
<td>60 GHz</td>
<td>60 GHz</td>
<td>60 GHz</td>
<td>60 GHz</td>
</tr>
<tr>
<td>IF Freq.</td>
<td>2 GHz</td>
<td>2 GHz</td>
<td>2 GHz</td>
<td>0</td>
</tr>
<tr>
<td>Conv. gain</td>
<td>1 dB</td>
<td>−2 dB</td>
<td>−11.6 dB</td>
<td>28* dB</td>
</tr>
<tr>
<td>LO Power</td>
<td>0 dBm</td>
<td>0 dBm</td>
<td>4 dBm</td>
<td>--</td>
</tr>
<tr>
<td>$P_{1dB}$</td>
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<td>−3.5 dBm</td>
<td>6 dBm</td>
<td>−22.5 dBm</td>
</tr>
<tr>
<td>Power diss.</td>
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<td>2.4 mW</td>
<td>--</td>
<td>9 mW</td>
</tr>
<tr>
<td>Area (mm$^2$)</td>
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<td>1.6 × 1.7</td>
<td>2.0 × 2.0</td>
<td>0.3 × 0.4**</td>
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* Voltage gain  ** Active area only (not include balun and DC & RF pads)
Figure 4.1: The circuit diagram of self-switching current-mode mixer.
Figure 4.2: The 4m+1-point analysis applied on HSPICE simulated of ac current gain.
Figure 4.3: circuit diagram of CMOS quadrature balanced current-mode mixer.
Figure 4.4: (a) Quarter-wavelength transmission line; (b) Shorted transmission line equivalent to the quarter-wavelength transmission line; (c) Coplanar waveguide.
Figure 4.5: The chip photograph of fabricated current-mod quadrature balanced down-conversion mixer.
Figure 4.6: The measurement setup for the diagram 60 GHz down-conversion mixer setup.
Figure 4.7: The measured and simulated IF output power versus RF input power.
Figure 4.8: The measured and simulated conversion gain versus LO power.
Figure 4.9: The measured LO-RF isolation characteristics.
Chapter 5

LOW–VOLTAGE CMOS CURRENT–MODE RECEIVER FRONT-END

Utilizing a standard 0.13μm 1P8M CMOS technology, a receiver front-end, local oscillator (LO), DC compensation are implemented for RF application at the 24-GHz industrial, scientific, medical band. The proposed receiver front-end is composed of transconductance low-noise amplifier (TLNA), RF current-mode mixer, IF current-mode mixers, DC–offset compensation, voltage control oscillator (VCO), and divide-by-two circuit. The TLNA proposed in chapter 3 of the thesis is used to amplified the RF input spectrum at 24 GHz with minimal noise contribution to enlarge the power difference between the received signal and noise, then the amplified RF input spectrum at 24 GHz is down-converted to an intermediate frequency (IF) of 8 GHz by using RF current-mode mixer proposed in chapter 4 of the thesis, and a follow-up IF current-mode mixers are used in-phase I and quadrature Q paths to directly convert the spectrum at IF frequency to zero frequency. The baseband signals are then applied to the DC–offset compensation circuit to eliminate DC–offset currents appear at the output of the IF current-mode mixer due to the self-mixing of the LO. The fabricated circuit in 0.13 – μm 1P8M CMOS technology demonstrates a conversion gain of 19.5 dB, and noise figure of 15 dB, while maintaining an input return loss better than –13 dB. The input-referred 1dB compression point of –25 dBm is measured. This receiver drains 35 mA from the supply voltage of 1 V.
This Chapter is organized as follows, Section 5.1 introduce the details of the operational principle and circuit implementation, the experimental results are demonstrated in Section 5.2. Finally, the summary is given in Section 5.3.

5.1 OPERATIONAL PRINCIPLE AND CIRCUIT IMPLEMENTATION

The block diagram of the designed 24-GHz receiver front-end is shown in Fig. 5.1. It is composed of a transconductance low noise amplifier (TLNA), RF current-mode mixer, IF current-mode mixers, DC–offset compensation, voltage control oscillator (VCO), and quadrature divided-by-two (QD2) circuit. The TLNA proposed in Chapter 3 is used to amplified the RF input spectrum at 24 GHz with minimal noise contribution to enlarge the power difference between the received signal and noise, then the amplified RF input spectrum at 24 GHz is down-converted to an intermediate frequency (IF) of 8 GHz by using RF current-mode mixer, and a follow-up IF current-mode mixers are used in-phase I and quadrature Q paths to directly convert the spectrum at IF frequency to zero frequency. The baseband signals are then applied to the DC–offset compensation circuit to eliminate DC–offset currents appear at the output of the IF current-mode mixer due to the self-mixing of the LO.

The heterodyne architecture of Fig. 5.1 greatly relaxes the requirement of high frequency quadrature LO signals. Thus on chip single oscillator VCO generates LO frequency at 16 GHz, and a follow-up quadrature divided-by-two circuit are used in this design. The detailed circuit designs and analyses are presented in the following.

5.1.1 TLNA

In the design of RF-CMOS LNAs, it is known that the key performance parameters are power-gain and noise figure (\(NF\)) besides the stability, linearity and isolation. The goal of LNA design is to achieve maximum power-gain and minimum \(NF\) simultaneously at any given amount of power dissipation. To reach this goal, the input impedance \(Z_{in}\) of a LNA must be kept close enough to the optimum source noise conjugate impedance \(Z_{n, opt}^*\).
The use of capacitive feedback matching network can achieve the above goal with a low-voltage. A schematic of the TLNA utilizing capacitive feedback matching network is shown in Fig. 5.2. Fig. 5.2 M1 with the input amplifier transistor and M2/M3 form the current-mirror amplifier as the second amplifier stage. The TLNA input capacitive impedance resonated out by L1 at the desired frequency. To provide capacitive load, a parallel resonance circuit composed of L2 and the parasitic capacitance at the drain of M1 $C_{out}$ is used, where the parallel resonance circuit resonates at the frequency below the operating frequency of the TLNA, in order to make it behave like a capacitive load. To ensure the stability of TLNA when the tank circuit at the drain of the M1 behaves like an inductor M6 is used. Due to the large impedance of the drain of M6 the quality factor of L2 is lowered. Thus, the feedback loop gain is small enough to quench any oscillation.

The biasing current of the TLNA is controlled by I1 through diode-connected transistors M5 and M7. C1 and C5 are dc blocking capacitors, while C2 and C4 are bypass capacitors. The tank circuit consists of L3 and C3 is used to resonate with the parasitic capacitances of the drain M3. R1 is used to provide the gate dc bias of M1, and chosen large enough that its equivalent noise current is small enough to be ignored. The condition for input impedance matching $Z_{in}$ is summarized as

$$Z_{in} = \frac{R_f}{(Q_f^2 + 1)} + \frac{1}{j\omega_o(C_{gs} + C_{gd})(\frac{1}{Q_f^2} + 1)}$$  \hspace{1cm} (5.1.1)

where

$$Q_f = \frac{\omega_o(C_{gs} + C_{gd})R_f}{g_m C_{gs}}$$  \hspace{1cm} (5.1.2)

$$R_f = \frac{C_{out}}{g_m C_{gd}}$$  \hspace{1cm} (5.1.3)

$g_m$ is the transconductance of M1, $C_{gd}$ is the gate-drain capacitance of M1, $C_{gs}$ is the gate-source capacitance of M1, and $\omega_o$ is the operating angular frequency. As it can be seen from the above equations, both $C_{gd}$ and $C_{out}$ with $g_m$ together providing a real term $R_f$ which contributes to the real input impedance in $Z_{in}$. They are called the capacitive feedback matching network.
5.1.2 RF Current–Mode Mixer

One may argue that a self-switching current-mode mixer proposed in Chapter 4 requires low operating power and gives high linearity. In addition, the gate node of switching devices is connected to Vdd, an AC ground, and the drain node is short-circuited at LO frequency, reducing the required LO power [78], which otherwise is a problem for high frequency mixers. However, the current-mode amplifier combiner is used to combine RF and LO signals instead of 90° branch-line hybrid coupler.

The concept of self-switching RF current-mode mixer is shown in Fig. 5.3. In Fig. 5.3 both RF signal current $i_{rf}$ and the LO signal current $i_{lo}$ are mirrored by $M_{n1}$ and $M_{p1}$ to $M_{n2}$ and $M_{p2}$, respectively. Due to the advantage of current-mode signal processing, the mirrored current signals are summed and fed to self-switching device $M_s$ by connecting the drains of $M_{n2}$ and $M_{p2}$ together. Under the assumption that $i_{lo}$ is much larger than $i_{rf}$, $M_s$ is switched on, when the mirrored $i_{lo}$ is high enough and in the direction of the source current $i_s$, and remains on only as long as this condition lasts, after which it is switched off. The parallel tank circuit ($C_T$ and $L_T$) at the drain of $M_s$ is used as bandpass filter to reject all signals except IF.

Normally, the single-ended mixer topology produces excessive LO-IF feedthrough, desensitizing the IF current-mode mixers tremendously. It also makes the signal path more susceptible to LO noise [80]. Therefore, the RF current-mode mixer in Fig. 5.3 is modified to a double-balance mixer topology with one RF input at ac ground as shown in Fig. 5.4. The RF current-mode mixer in Fig. 5.4 downconverts the RF input spectrum from 24 GHz to an IF 8 GHz. The drain current of $M_3$ $i_{rf}$ from the TLNA is fed into the low-impedance diode-connected transistor $M_8$, and amplified by current-mirror amplifiers $M_8/M_{12}$ and $M_8/M_{13}$. $M_{20}$, $M_{21}$, $M_{22}$, and $M_{23}$ are the self-switching devices. The two parallel LC resonate tanks ($L_4$, $C_{10}$) and ($L_5$, $C_9$) are used to select the IF frequency at 8 GHz. In order to improve the conversion gain of the RF current-mode mixer and reduce the mismatch between the switching pairs ($M_{20}$, $M_{21}$) and ($M_{22}$, $M_{23}$) center tapped inductors $L_6$ and $L_7$ are used. The LO differential currents ($i_{lo+}$,$i_{lo-}$) are fed through current-mirror $M_{14}$/M_{16},M_{18} and $M_{15}$/M_{19},M_{17}, respectively. To prevent the LO-IF feedthrough, $C_9$ is used to connect one of the RF input of the mixer to an ac ground. In order to increase the
image rejection of the circuit. A series tank circuit consisting of L8 and C8 resonates at 8 GHz, employing notch filter and posting the overall simulated image rejection to more than 49 dB as shown in Fig. 5.5.

5.1.3 IF Current–Mode Mixer

To relax the stake problem in the conventional CMOS Gilbert cell and lower the power supply voltage a differential current $i_{if}$ inputs are fed to IF current-mode mixers circuit instead of voltage [81]. The RF current-mode mixer in the proposed receiver must drive two IF current-mode mixers to produce quadrature outputs. This is realized with a differential RF currents fed to the tails of two differential pairs current-multiplier devices in parallel, which together comprise two double balance mixers as shown in Fig. 5.6. The two pairs on the left (M29-M32) are fed by one phase of the differential divider current ($i_{LOQ}^+$ and $i_{LOQ}^-$) through diode-connected devices (M37 and M38), and the two pairs on the right (M33-M36) are fed by its quadrature phase ($i_{LOI}^+$ and $i_{LOI}^-$) through diode-connected devices (M39 and M40). The output current signals are cross-coupled and fed to DC–offset compensation stage. Thus, the differential outputs ($i_{Q}^+$ and $i_{Q}^-$) and ($i_{l}^+$ and $i_{l}^-$) are the desired downconverted signals in quadrature phase. To further maximize the voltage headroom the biasing current source is implemented as parallel resonating tank circuit (L9,C12) and (L10, C11). The biased currents of IF current-mode mixers are controlled by $I_{refL}$ and $I_{refR}$, where $I_{refL}$ and $I_{refR}$ are mirrored through M41 and M46 to M37-M38 and M44-M45.

If all MOSFET devices are in the saturation region, the multiplication gain of the left IF current-mode mixer, which is identical to the right IF current-mode mixer, can be derived as following

$$
\frac{(I_{Q}^+ - I_{Q}^-)}{A_f} = (I_{M29} + I_{M31}) - (I_{M30} + I_{M32})
$$

(5.1.4)

where $A_f$ is the current gain of the DC–offset compensation circuit. By defining $I_1$ and $I_2$
as

\[ I_1 = I_{M29} + I_{M30} \]  
\[ I_2 = I_{M31} + I_{M32} \]  

(5.1.5) (5.1.6)

(5.1.4) can be re-written as

\[ \frac{(I_{Q+} - I_{Q-})}{A_I} = (I_1 + I_2) - 2(I_{M30} + I_{M32}) \]  

(5.1.7)

(5.1.7) can be farther simplified by using the following current mirror propriety

\[ \frac{I_{M38}}{I_{M37}} = \frac{I_{M29}}{I_{M30}} = \frac{I_{M32}}{I_{M31}} \]  

(5.1.8)

in (5.1.7), solving \( I_{M30} \) and \( I_{M32} \) in terms of \( I_{M38} \), \( I_{M37} \), \( I_1 \), and \( I_2 \). (5.1.7) can be re-expressed as

\[ \frac{(I_{Q+} - I_{Q-})}{A_I} = \frac{(I_2 - I_1)(I_{M37} - I_{M38})}{(I_{M37} + I_{M38})} \]  

(5.1.9)

However, the summation of \( I_{M37} \) and \( I_{M38} \) is equal to \( 2I_{ref} \), while their subtraction is equal to \( \Delta Q \) (\( \Delta Q = i_{LOQ+} - i_{LOQ-} \)), and \( (I_2 - I_1) \) is equal to \( \frac{1}{2} \Delta i_{if} \), where \( \Delta i_{if} = i_{r+f+} - i_{r+f-} \). Thus, the differential output currents are given as

\[ (I_{Q+} - I_{Q-}) = A_I \frac{\Delta i_{if} \Delta Q}{4I_{ref}} \]  

(5.1.10)

5.1.4 DC–Offset Compensation Circuit

The purpose of the DC–offset compensation circuit is to reduce DC–offssets due to self-mixing. The proposed DC–offset compensation is shown in Fig. 5.7, which consists of a current-mirror amplifier M47/M54, and negative feedback loop with a low pass filter (LPF) enclosed by the dash box. In the circuit enclosed by the dash box in Fig. 5.7, the DC–offset current results from self-mixing is sensed by M50, and mirrored by M53 to the rectifier circuit (M52, C13), a DC voltage corresponding to the DC–offset current will be stored in C13. This voltage is applied to the gate of M51 to generate offset correction current, the offset correction current are mirrored to M48 through M49. As a result, the offset correction current are injected back, Therefore, the DC–offset current in IF current-mode
mixer is adjusted leading to the compensation of offset current in the IF current-mode mixer.

In addition, the circuit enclosed by the dash box help to lower the required power for current-mirror M47/M54 to amplifies the baseband signal. Assume a prefect device match and neglect the effect of channel length modulation. The biasing current of M54 is

\[ I_{M54} = A_c I_a \] (5.1.11)

Where \( A_c \) is the current gain of current-mirror amplifier M47/M54, and \( I_a \) is the biasing DC current of M54 (\( I_{M54} \)). \( I_a \) is given as

\[ I_a = \frac{I_{in}}{(B + 1)} \] (5.1.12)

Where \( I_{in} \) is the input biasing DC current of the DC–offset compensation circuit, B is the current ratio between the biasing DC current of M47 (\( I_{M47} \)) and M48 (\( I_{M48} \)), substituting (5.1.11) in (5.1.12)

\[ I_{M54} = \frac{I_{in} A_c}{(B + 1)} \] (5.1.13)

From (5.1.11), the required DC current of M54 (\( I_{M54} \)) is reduced by a factor of \((1 + B)\) while the current gain keeps equal to \( A_c \). The sensitivity of the rectifier circuit to the variation of the M52 width (\( W_{M52} \)) is shown in Fig. 5.8, where the cut–off frequency of DC–offset compensation circuit weak dependents on the width variation of M52 (\( W_{M52} \)).

### 5.1.5 VCO and Divider

For the purposes of testing, a high performance VCO with quadrature divided-by-two operating at 16 GHz and 8 GHz, respectively are integrated. The schematic of the proposed VCO and quadrature divided-by-two circuit are shown in Fig. 5.9. The core structure of the VCO in Fig. 5.9 consists of cross-coupled transistors M56 and M55 with center tap inducer L11. In order to provide tuning capabilities varactors C14 and C15 are used, where the oscillation frequency of VCO is controlled by voltage V1. The quadrature divided-by-two circuit is consists of two pairs of cross-coupled transistors M57-M58 and M59-M60 with two center tap inductors L12 and L13. To increase the locking range varactors C18-C19 and C17-C16 are used, and controlled by voltage V2. In the VCO topology, the bias current is
defined by current source $I_{vco}$, which mirrored through M64 to the tail transistor M63 for a stable output power level.

5.2 Experimental Results

The designed 24-GHz current-mode receiver front-end circuit was fabricated in 0.13−μm 1P8M CMOS technology. The top metal of this process is with the thickness of 3.35 μm. The equivalent relative dielectric constant $\varepsilon_{eff}$ is about 4.2. Based on the technology information of the backend process, the electromagnetic (EM) tool HFSS is used to evaluate and extract the characteristics of the interconnections within the circuits as shown in Fig. 5.10.

The floor plans of the proposed receiver front-end are depicted in Fig. 5.11. Four on-chip octagonal spiral inductors, and seven center tap octagonal inducer are used. The distances of each inductor are more than 100 μm to mitigate the magnetic coupling between on-chip inductors. In addition, the distances of the active devices of TLNA, RF current-mode mixer, IF current-mode mixer, DC−offset compensation circuit, VCO, and quadrature divided-by-two circuits are arranged far, the noise influence between these circuits are kept small. The signal path between input pad and the input of the TLNA is drawn as short as possible to avoid additional signal losses and increase of NF. Besides, large on-chip decoupling capacitors are used between the biases and ground, such that high frequency noises can be bypassed to ground and consequently stable biases and supplies of the receiver can be achieved. The performance of each circuit block in this 24-GHz current-mode receiver is over-designed to overcome process variations. This chip occupies the active region of 1.850 × 1.806 mm$^2$ including testing pads.

The measurement setups of this fabricated receiver are described as follows. The on-wafer probing measurement is adopted to verify the performance of the receiver frontend. One GSG RF probes with the pitch of 100 μm, two GSGSG RF probes with the pitch of 150 μm, and a 12-pin dc probe with the pitch of 150 μm are applied to probe the testing pads. The S parameters are measured to analyze the input matching characteristics by the network analyzer. To measure conversion gain and linearity, two signal generators are used to provide a RF and a LO signals for the device under test (DUT). The spectrum analyzer
is used to monitor the spectrum to verify the linearity and conversion gain of the receiver. The NF analyzer with a broadband noise source is used to measure the performance of NF of the receiver. Owing to the frequency shift of the VCO in fabricated chip, the laser cut is used to modify operational frequency of the VCO. Moreover, the measured current consumption of the receiver is 35 mA from the supply voltage of 1 V.

From Fig. 5.12 the measured and simulated input reflection coefficient of the proposed receiver is better than $-13\,\text{db}$, Fig. 5.13 presents the measured gain and $\text{NF}$ versus RF input frequency. The losses from cables, probes and adaptors are compensated. Moreover, the LO is set to the frequency of 16 GHz, and the the output is observed at the fixed IF frequency of 100 MHz. The measured conversion gain of the RF frequency is 19.5 dB, while the $\text{NF}$ is 15 $\text{dB}$. In addition, due to DC–offset compensation circuit, when the input RF at 24 GHz the gain of 10.5 is measured. Thus, The DC–offset compensation circuit reduces the DC gain by 10 dB. The measured output power versus the input power is shown in Fig. 5.14 where the input referred 1-$\text{dB}$ compression gain is $-25\,\text{dBm}$.

The measured output frequency of VCO versus control voltage $V_1$ from 0 to 1 is measured by the observation of the VCO leakage from IF output port. It can be seen from Fig. 5.15 that the VCO output frequency is shift to lower frequency about 2-GHz. Because the model of the two-turn symmetric inductor is calculated by the interpolation from one-turn and three-turn symmetric inductors, the accuracy of the interpolation method is verified by the 3D EM CAD tools HFSS. The whole EM simulation result can be closer to measurement result with frequency offset of 0.5 GHz. In order to measure the receiver in the desired band, laser-cut technique is adopted to cut off a part of the varactors. Thus, the varactors at each output terminals of VCO and quadrature divided-by-two are reduced so that the oscillation frequency of the VCO is shifted upward. After coping with several tested chips with this procedure, a resultant oscillation frequency tuned from 15 GHz to 16.5 GHz under a tuning voltage of 0 V to 1 V. The microphotograph of the VCO and quadrature divided-by-two circuits after laser-cut is shown in Fig. 5.16.

Table 5.1 summaries the performance of the proposed current-mode receiver front-end. In addition, some comparison results of published 24-GHz receiver front-end circuits are also provided. Compared to the works published in [61], [31], and [82]. The proposed
24-GHz CMOS current-mode receiver front-end has the advantage of high level of integration with smaller power dissipations and can be operated under low-voltage with a good linearity performance.

5.3 Summary

In this chapter, the current-mode design techniques of CMOS RF circuits are developed and are applied to realize the 24-GHz CMOS current-mode receiver front-end. The receiver integrated with TLNA, RF current-mode mixer, IF current-mode mixer, DC-offset compensation circuit, VCO, and quadrature divided-by-two circuits. The TLNA proposed in chapter 3 of the thesis is used to amplified the RF input spectrum at 24 GHz with minimal noise contribution to enlarge the power difference between the received signal and noise, then the amplified RF input spectrum at 24 GHz is down-converted to an intermediate frequency (IF) of 8 GHz by using RF current-mode mixer proposed in chapter 4 of the thesis, and a follow-up IF current-mode mixers are used in-phase I and quadrature Q paths to directly convert the spectrum at IF frequency to zero frequency. The baseband signals are then applied to the DC-offset compensation circuit to eliminate DC-offset currents appear at the output of the IF current-mode mixer due to the self-mixing of the LO. The fabricated circuit demonstrates a conversion gain of 19.5 dB and noise figure of 15 dB while maintaining an input return loss better than −13 dB. The input-referred 1dB compression point of −25 dBm is measured. This receiver drains 35 mA from the supply voltage of 1 V.
Table 5.1: The measured performances and comparisons results of published 24-GHz receiver front-end circuits.

<table>
<thead>
<tr>
<th>Tech.</th>
<th>This work</th>
<th>[61]</th>
<th>[31]</th>
<th>[82]</th>
</tr>
</thead>
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<tr>
<td>Level of</td>
<td>LNA, double-balance RF mixer</td>
<td>0.13μm CMOS</td>
<td>0.18μm CMOS</td>
<td>0.18μm CMOS</td>
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<tr>
<td>Integration</td>
<td>I/Q differential IF mixer, DC-offset compensation, VCO with quadrature divider</td>
<td>3-stage LNA</td>
<td>3-stage LNA</td>
<td>3-stage LNA</td>
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<td>Topology</td>
<td>Current-mode</td>
<td>Voltage-mode</td>
<td>Voltage-mode</td>
<td>Current-mode</td>
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<td>21.8</td>
<td>24</td>
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<tr>
<td>$Freq_{LO}$ [GHz]</td>
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<td>16.9</td>
<td>19.18</td>
<td>19</td>
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<tr>
<td>$Freq_{IF}$ [GHz]</td>
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<td>4.82</td>
<td>5</td>
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<tr>
<td>$Gain_{RX}$ [dB]</td>
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<td>27.5</td>
<td>28.4</td>
<td>12</td>
</tr>
<tr>
<td>$NF_{RX}$ [dB]</td>
<td>15(6**)</td>
<td>8</td>
<td>6</td>
<td>13.3</td>
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<tr>
<td>$P_{1dB}$ [dBm]</td>
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<td>-23</td>
<td>-23.2</td>
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<tr>
<td>Image Rejection [dB]</td>
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<td>31</td>
<td>44.8</td>
<td>–</td>
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<tr>
<td>Power [mW]</td>
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<td>49.8</td>
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<tr>
<td>supply [V]</td>
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<td>1.5</td>
<td>1.8</td>
<td>1.2</td>
</tr>
<tr>
<td>Chip area [$mm^2$]</td>
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<td>0.4 × 0.5</td>
<td>1.1 × 1.2</td>
<td>1.45 × 0.72</td>
</tr>
</tbody>
</table>

* on-chip VCO.
** the simulated NF of LNA and RF current-mode mixer.
Figure 5.1: The block diagram of the 24-GHz current-mode receiver front-end.
Figure 5.2: The circuit diagram of the TLNA.
Figure 5.3: The simplified circuit diagram of the self-switching current-mode RF current-mode mixer.
Figure 5.4: The circuit diagram of the double-balance self-switching current-mode RF current-mode mixer.
Figure 5.5: The simulated gain of TLNA with and without notch filter.
Figure 5.6: The circuit diagram of the quadrature IF current-mode mixers.
Figure 5.7: The circuit diagram of DC–offset compensation circuit.
Figure 5.8: The sensitivity of the rectifier circuit to the variation of the M52 width.
Figure 5.9: The circuit diagram of VCO with quadrature divided-by-two circuit.
Figure 5.10: The interconnections within the circuits in the receiver are simulated by HFSS.
Figure 5.11: The chip micrograph of the fabricated current-mode receiver front-end.
Figure 5.12: The measured and simulated input reflection coefficient of the proposed receiver.
Figure 5.13: The measured gain and $NF$ of the proposed receiver.
Figure 5.14: The receiver measurement results of $P_{\text{in}}$ versus $P_{\text{out}}$. 
Figure 5.15: The measured and simulated tuning range of the VCO.
Figure 5.16: The microphotograph of the VCO and quadrature divided-by-two circuits after laser-cut.
Chapter 6

CONCLUSIONS AND FUTURE WORKS

6.1 Main Results of This Dissertation

In this thesis, the design methodologies and implementation techniques of low-voltage current-mode RF front-end circuits are presented.

first, a new input impedance power matching technique for LNA is proposed and analyzed. In the proposed technique, the gate-drain capacitor of the input common-source amplifier and the capacitive feedback matching network are used to implement a real input impedance in order to match with the input source impedance. Thus, the technique is called technique of capacitive feedback matching network. By using this technique, the minimum noise figure and maximum power gain can be achieve simultaneously, furthermore, it can be used with very low supply voltage without degraded the linearity. The full noise analysis of LNA utilizing the proposed technique is supported by mathematical derivations and it is complemented and validated by measurements. Where, the proposed LNA which is implemented in a 0.18 − μm 1P6M CMOS technology is operated at the frequency of 12.8 GHz. It has a gain S21 of 13.2 dB, a noise figure (NF) of 4.57 dB and an NFmin of 4.46 dB. The reverse isolation S12 of the LNA can achieve −40 dB and the input and output return losses are better than −11 dB. The input 1-dB compression point is −11 dBm and IIP3 is −0.5 dBm. This LNA drains 10 mA from the supply voltage of 1 V.
Secondly, mm-wave RF CMOS low LO-power quadrature balanced self-switching current-mode mixer is proposed. The mixer consists of common-gate amplifier as input stage, an area efficient 90-degree branch-line hybrid coupler, and CMOS self-switching current-mode devices, the 90-degree branch-line hybrid coupler is designed to deal with the issue on the combination of RF and LO signals at very high-frequency, in order to implement area efficient 90-degree branch-line hybrid coupler, the branch-line and the through-line lengths of the hybrid are reduced from $\lambda/4$ to $\lambda/6.4$ and $\lambda/10$, respectively, based on the methodology of a high-impedance coplanar waveguide with shunt lumped capacitors. The proposed mixer, using 0.13 $\mu$m 1P8M CMOS technology, can down-convert 60 $GHz$ RF signal to 2 $GHz$ intermediate frequency (IF) signal, with a LO power of 0 $dBm$ at 58GHz. In the design, the mixer had a single-end conversion gain of 1 $dB$ and an input-referred 1$dB$ compression point of 2 $dBm$. The LO-RF isolation of the mixer can achieve $-37$ $dB$ while using 3 mA from a supply voltage of 1.2 V.

Finally, Industrial-Science-Medical (ISM) receiver operates at 24 GHz is proposed. The receiver consists of TLNA, RF current-mode mixer, IF current-mode mixers, DC offset compensation, voltage control oscillator (VCO), and quadrature divided-by-two circuit. The TLNA proposed in the first part of the thesis is used to amplified the RF input spectrum at 24 GHz with minimal noise contribution to enlarge the power difference between the received signal and noise, then the amplified RF input spectrum at 24 GHz is down-converted to an intermediate frequency (IF) of 8 GHz by using RF current-mode mixer proposed in the second part of the thesis, and a follow-up IF current-mode mixers are used in-phase I and quadrature Q paths to directly convert the spectrum at IF frequency to zero frequency. The baseband signals are then applied to the DC offset compensation circuit to eliminate DC offset currents appear at the output of the IF mixer due to the self-mixing of the LO. The fabricated circuit in 0.13 $\mu$m 1P8M CMOS technology demonstrates a conversion gain of 19.5 $dB$, and noise figure of 15 $dB$, while maintaining an input return loss better than $-13$ $dB$. The input-referred 1$dB$ compression point of $-25$ $dBm$ is measured. This receiver drains 35 mA from the supply voltage of 1 V.

The noise figure and power consumption of the LNA utilizing can be further reducing by study the power noise optimization techencys which applied on common-sorource inductive deguratin and abpleide to
In summary, the advance in CMOS technology has reduced the operational supply voltage of MOSFETs and increasing its unit-gain frequency, it is quite challengeable to design high-performance high-frequency low-voltage high-integration receiver front-ends by using the advance CMOS technology, and integrate them with the baseband signal processing VLSI. Thus, in order to design low-voltage CMOS receiver front-end at 24 GHz, both capacitive feedback matching network technique and current-mode methodology are developed and analyzed.

### 6.2 Future Works

The simulation and measurement results have shown that the current-mode front-end receiver can achieve good performance under low-voltage supply. The low power dissipation of the receiver offer interesting possibilities for higher performance. For example, suppose the topology of two antennas with two integrated current-mode receivers. Even without sophisticated antenna diversity and beam forming techniques, the baseband current signal of the two receivers can be added to improve the signal-to-noise ratio by 3 dB. Note that phase coherence at the two antennas (at 24 GHz) is not critical; only the baseband data streams must have a reasonable phase alignment. However, the DC biasing of the proposed receiver increase its complicity. Thus, it is required to design a DC biasing circuit such as constant-gm bias circuit. This can reduces the sensitivity of the proposed receiver for temperature and process variations and increase the performance of the receiver.

In the capacitive feedback matching network LNA, the difference between noise figure and minimum noise figure are slightly different and instinctive for operational frequency shift. Even FOM of the proposed LNA is excellent in comparison with other proposed LNAs, it still can be increased. To achieve higher FOM, the noise-power optimization techniques for conventional inductive degeneration common-source can be adopted.

In the implementation of self-switching current-mode mixer, to reduce the mismatch between the self-switching device due to the fabrication process, the current though the self-switching devices of the mixer can be adjusted by feedback signals measured from drain or source of the self-switching device. Furthermore, to efficiently combine the IF-branches of the mixer, a follow-up $2 - GHz$ IF amplifier can be used. Future research will
be conducted to design a complete 60–GHz CMOS current-mode front-end receiver using the proposed mixer and LNA.
Figure 6.1: National Chiao Tung University on-waver probe analytical station test setup 2008.
Appendix A

As can be seen from Fig. 4.2, $A_i$ can be represented by $4m+1$ points, Thus, by using the Riemann sum [83] to approximate the integration in (4.1.4) when $j = 1$, (4.1.4) can be approximated as

$$A_{cl} = \frac{1}{2\pi} \int_0^{2\pi} A_i \sin(\omega_{LO}t) d(\omega_{LO}t) \approx \sum_{P=-2m}^{2m} F(X_P) \Delta X,$$  \hspace{1cm} (A.0.1)

where

$$F(X_P) = \frac{1}{2\pi} C_P \sin(P \frac{\pi}{2m}),$$  \hspace{1cm} (A.0.2)

$$\Delta X = \frac{\pi}{2m}.$$  \hspace{1cm} (A.0.3)

In the above equations, $C_P$ is the value of $A_i$, which corresponds to the LO current equal $I_0 \sin(P \frac{\pi}{2m})$. Substituting (A.0.2) and (A.0.3) in (A.0.1), $A_{cl}$ can be rewritten as

$$A_{cl} \approx \frac{1}{4m} \sum_{P=-2m}^{2m} C_P \sin(P \frac{\pi}{2m}).$$  \hspace{1cm} (A.0.4)

For sine wave input LO, the above equation can be farther simplified as

$$A_{cl} \approx \frac{1}{4m} \left[ \sum_{P=-2m}^{0} C_P \sin(P \frac{\pi}{2m}) + \sum_{P=1}^{2m} C_P \sin(P \frac{\pi}{2m}) \right]$$  \hspace{1cm} (A.0.5)

$$= \frac{1}{4m} \left[ (C_m - C_{-m}) + 2 \sum_{P=-m+1}^{-1} C_P \sin(P \frac{\pi}{2m}) + 2 \sum_{P=1}^{m-1} C_P \sin(P \frac{\pi}{2m}) \right]$$  \hspace{1cm} (A.0.6)

by rearranging the index of summation of the first partial sum.
\[ \sum_{p=-m+1}^{-1} C_p \sin\left(\frac{P \pi}{2m}\right) = -\sum_{p=1}^{m-1} C_{-p} \sin\left(\frac{P \pi}{2m}\right) \quad (A.0.7) \]

Therefore, by substituting (A.0.7) in (A.0.6), the first harmonic conversion gain can approximated as

\[ A_{c1} \approx \frac{1}{4m} \left[ (C_m - C_{-m}) + 2 \sum_{p=1}^{m-1} (C_p - C_{-p}) \sin\left(\frac{P \pi}{2m}\right) \right] \quad (A.0.8) \]
Bibliography


