Chapter 4
Experimental Results and Discussions

The device process steps for the InAlP HEMT and schottky diode fabrications are described and the experimental results including I-V characteristics, C-V characteristics and TEM, EDX, XRD analysis data are presented. Device with different schottky metal systems, such as Ti/Pt/Au, Pt/Ti/Pt/Au and W/Ti/Pt/Au were also fabricated and characterized under different treatments for performance and stability comparisons.

4.1 Mesa Isolation

Mesa etching was tried using one and three steps, HF:H₂O₂:H₂O was used for one step etching and for three-step etch, we use HF:H₂O₂:H₂O to etch GaAs/InGaAs/AlGaAs and HCl:H₂O to selective etch AlInP layer. The etch depth was measured by α-stepper. The etchants were used to etch away the epi-layers down the middle of the buffer layer. The total thickness of the active layers is about 4000Å. The edge profile of the mesa is important and must be tuned to avoid the discontinuity of the ohmic pads across the mesa edge. Mesa profile using one step etch is shown in Figure 4.1(a). Mesa profile using three steps is shown in Figure 4.1(b). From SEM photos, the edge profile using one step etch is suitable for metal stepover. One-step etch is simple and will be applied to the device fabrication.

4.2 Ohmic contact fabrication

After mesa isolation, ohmic metals (Au/Ge/Ni/Au) were deposited by E-gun evaporation and followed by rapid thermal annealing (RTA) at different temperatures. In order to get lower contact resistance, different
annealing temperatures were treated and the relationship of the contact resistances at different annealing temperatures are shown in Figure 4.2(a). From this figure, the contact resistances at different temperatures were still very high. We try to use another ohmic metal system Ge/Au/Ni/Ti/Au (700/1400/500/200/1000A). The results of the contact resistances at different annealing temperatures are shown in Figure 4.2(b). The lowest contact resistance achieved was $5 \times 10^{-7} \Omega \cdot \text{cm}$ after RTA at 450°C for 30 seconds with forming gas of 15% hydrogen and 85% nitrogen.

4.3 Optical gate

A process for fabricating submicron T-shaped gate using deep-UV lithography has been developed. Tri-layer resist system with LO/HI/LO sensitivity was used to provide T-shaped resist cavity with undercut profile and submicron footprint. It has been shown that submicron T-shaped profile suitable for lift off process can be obtained by the use of PMMA/P(MMA-MAA)/PMMA resist system. A 0.5 μm T-shaped gate has been fabricated using this technique. The cross-section of the T-gate was shown in Figure 4.3(a). In order to increase the yield of the process and get shorter gate length, LO/HI sensitivity bilayer resist system was used for gate fabrication. The sensitivity of PMMA to DUV is lower than the sensitivity of the P(MMA-MAA), so the opening for PMMA and P(MMA-MAA) that were developed by MIBK(Methyl-iso-butylketon) and IPA(isopropyl alcohol) solution is different. It is shown that an undercut submicron profile for easy lift off can be obtained by the use of PMMA/P(MMA/MAA) bilayer resist structure. A 0.38 μm gate has been
fabricated using this technique. Figure 4.3(b) shows the SEM micrograph of the bilayer resist profile. This process was successfully applied to the fabrication of AlInP PHEMTs. The process is with high throughput and low cost and is an alternative to E-beam lithography.

4.4 Selective etching in gate recess and Gate metallization

Gate recess is the most critical process for the GaAs FET fabrication. The gate recess process is to etch a gate slot in the gate area and contact to the schottky layer before gate deposition. The depth of the gate recess is an important parameter for the device performance, so accurately controlled gate recess is necessary. However, it is very difficult to control the gate recess process, because the cap and schottky layer are very thin and the source-to-drain current decreases very fast during gate recess process. Selective etching for gate recess was done by using etching solution with a higher etching rate on the cap layer ($n^+\text{GaAs}$) and a lower etching rate on the schottky layer (AlInP). Figure 4.4 shows the etching depth vs time of $n^+\text{GaAs}$ and AlInP in CA/$\text{H}_2\text{O}_2$. The figure shows that the etching selectivity between GaAs and InAlP is high.

After the recess etching, the gate metal Ti/Pt/Au (600/600/1800A) were deposited by E-gun evaporation system. After evaporation, the wafer was immersed into ACE for lift-off, then rinsed in IPA and blown dry by nitrogen for cleaning. Finally, OM was used to inspect the surface of the device, and the passivation process was performed to protect the surface of the devices.

4.5 InAlP Schottky Diodes
4.5.1 The Ti/Pt/Au/InAlP Schottky Metal Structures

4.5.1-a Interfacial Properties of Ti/Pt/Au Schottky Contact

The interfacial structure was investigated by XRD. Figure 4.5.1-1 shows XRD results of the Ti/Pt/Au schottky contact samples before and after annealing. Strong Ti (101), Pt(111) and Au (111) peaks were observed, and Ti (101), Pt(111) and Au (111) peaks were observed in the as-deposited and annealed samples. There was no compound formation after 200°C for 30 minutes annealing. The Al$_2$Ti(022) peak appeared after annealing at 300°C for 30 minutes. Al$_2$Ti(211), AlTi(220), AlTi(200), AlTi(002), Al$_2$Ti(017) compound appeared after annealing at 400°C for 30 minutes and Al$_2$Ti(022) peak disappears. AlTi(002) and Al$_2$Ti(017) compound appeared after annealing at 500°C for 30 minutes.

4.5.1-b Characteristic of Ti/Pt/Au Schottky contact

Figure 4.5.1-2 shows the current-voltage (I-V) characteristic of the Ti/Pt/Au schottky diode. It is clear from the plot that high temperature annealing degrades the diode characteristics and increases the reverse leakage current. The observed ‘softening’ of the reverse I-V characteristic is believed to be the diffusion of Ti into InAlP layer. The gate leakage current reaches the highest of 4×10$^{-6}$ A after annealed at 400°C for 30 minutes and after annealed at 500°C for 30 minutes, the I-V curve shifted positive, the leakage current at 0 V is not the lowest, this may be due to the deep diffusion of the schottky metal into the InAlP layer, the carrier tunnel
effect occurs. Figure 4.5.1-3 shows the forward current for Ti/Pt/Au contact annealed at different temperatures. It shows little change after annealing at 200°C for 30 minutes but upon annealing at 300°C, 400°C, 500°C, an increase in forward current was observed. The increase in conduction is most pounced after annealing at 400°C is due to the high leakage current, and this increase in conduction was associated with the degradation of the diode. Figure 4.5.1-4&Figure 4.5.1-5 show ideality factor and schottky barrier height after different annealing temperature. It is clear from the plots that high temperature annealing increased ideality factor and reduced the schottky barrier height. This schottky characteristics degradation for the diodes is attributed to the diffusion of Ti into InAlP layer. The Schottky barrier heights estimated by the measured I-V curves of the diodes were 0.83eV, 0.78 eV, 0.73 eV, 0.53 eV and 0.66 eV, the estimated ideality factor were 1.51, 1.77, 1.84, 2.13, 1.56 for the as-deposited, 200°C, 300°C, and 400°C, 500°C samples respectively. The reaction of Ti and Al resulted in the formation of TiAl and TiAl₂, which resulted in the continual decrease in barrier height, and the increase in ideality factor. The sharp increase of the ideality factor and decrease of the schottky barrier height after annealed at 400°C may be due to the TiAl, TiAl₂ compound formation in the interface after annealing. The measured breakdown voltages were 19.5V, 19.5V, 20V, 22.5V and 22V, for as-deposited, 200°C, and 300°C, 400°C and 500°C samples respectively as shown in Figure 4.5.1-6.

4.5.1-c C-V measurement of Ti/Pt/Au Schottky contact
The Schottky diode samples with a diameter of 0.05 mm were annealed at different temperatures for C-V measurements. The C-V characteristic of the diode is sensitive to the diffusion depth so that the junction capacitance was measured by applying voltage sweep between 0 to -1V with testing signal at 1 MHz. Ti inter-diffusion reduces the separation of the Ti metal in Ti/Pt/Au gate metal stacks and InGaAs channel. Figure 4.5.1-7 shows the capacitance-voltage characteristics after annealed at different temperatures. It shows that the curves shift positive with higher annealing temperatures. The positive shift of the C-V curves originates from the metal diffusion and is associated with the increase of the threshold voltage in HEMT devices. It showed no increase in the C-V curve after the sample was annealed at 500 ℃ for 30 minutes. This may be due to the deep diffusion of Ti into InAlP layer. The changes in the device parameters, such as gate capacitance and threshold voltage shift, can constitute serious problems in the design and fabrication of integrated circuits if the gate process is not well controlled.

4.5.1-d Sheet resistance of Ti/Pt/Au Schottky contact

The sheet resistance of Ti/Pt/Au was measured by four-point probe. The sheet resistances of these structures were shown in Figure 4.5.1-8. It was found that the sheet resistance of the film increased with higher temperature. When the samples were annealed from room temperature to 400 ℃, the sheet resistance slowly increased to 22.72 mΩ/□ after annealing at 300 ℃ for 30 minutes, and then increased sharply after 400 ℃ annealing for 30 minutes. Therefore, it seems that the enlargement of Ti grains and
the increase of defects were most likely the causes of the increase in the sheet resistance. The sharp change in the sheet resistance at 400°C for 30 minutes was mainly due to the formation of intermetallic compounds or the over-alloy of the metal.

4.5.1-e TEM image of the annealed Ti/Pt/Au sample after thermal annealing

Figure 4.5.1-9 shows a TEM image of Ti/Pt/Au contact on InAlP epitaxial structure after annealing at 400°C for 30 minutes. It shows compound formation at the InAlP layer so that the leakage current annealed at 400°C was high. Figure 4.5.1-10 shows the physical evidence of Ti inter-diffusion into the InAlP schottky barrier layer. Ti diffused into the InAlP layer and some compounds were observed at the interface. The EDX spectrum on EDX point 1 in Figure 4.5.1-11 was shown in Figure 4.5.1-12. The analysis of EDX point 2 and 3 (in Figure 4.5.1-13, 4.5.1-14) confirm that Ti sinking into the InAlP layer but not into the InGaAs channel. And there were no traces of Pt and Au signals. These results substantiate that gate metal sinking in InAlP PHEMTs is the primary degradation mechanism. The schottky diode degradation exhibits an increase in reverse gate leakage current, sheet resistance, and a decrease in the schottky barrier height.

4.5.2 The Pt/Ti/Pt/Au/InAlP Schottky Metals Structures

4.5.2-a Characteristics of Pt/Ti/Pt/Au schottky contact
The current-voltage (I-V) characteristics of the diodes after thermal annealing are shown in Figure 4.5.2-2. The leakage current reduced after annealing at 200°C for 30 minutes, however, after annealing at 300°C for 30 minutes, the leakage current increased about 10 times than that of the 200°C annealed sample. The curve shifts positive after annealing at 300°C for 30 minutes, this may be due to the diffusion of Pt deep into the InAlP layer. Figure 4.5.2-3 shows the forward current for the Pt/Ti/Pt/Au contact after annealed at different temperatures. An increase in forward current was observed. The increase in diode conduction upon annealing was associated with the degradation of the diode, but the degradation of the turn on voltage was little compared with that of the Ti/Pt/Au contact, which may be due to the balance of schottky barrier height increase and the degradation caused by the metal diffusion. Figure 4.5.2-4&4.5.2-5 shows the ideality factor and schottky barrier height of Pt/Ti/Pt/Au contact annealed at different temperatures. The Schottky barrier heights estimated by the measured I-V curves of the diodes were 0.64 eV, 0.7 eV, 0.78 eV, 0.86 eV and 0.81 eV, the estimated ideality factor were 2.64, 2.58, 1.64, 1.26, 1.51 for as-deposited, 200°C, 300°C, and 400°C, 500°C samples respectively. Schottky barrier height rises to the highest level of 0.86 eV after the annealing at 400°C. The increase of schottky barrier height and decrease of ideality factor may be due to the intermetallic compound formation or the decrease of distance between Pt and InAlP caused by Pt inter-diffusion. The breakdown voltage was defined as the applied voltage when leakage current was 0.002A. Figure 4.5.2-6 shows the reverse breakdown voltage
of Pt/Ti/Pt/Au contact at different annealing temperatures. The measured breakdown voltages were 23V, 20V, 20.2V, 19V and 18V, for as-deposited, 200°C, and 300°C, 400°C and 500°C samples respectively. After annealing, the breakdown voltage decreased due to the Pt diffused closer to the InGaAs channel layer. Therefore, Pt diffusion into the Schottky layer increases the gate leakage current.

4.5.2-b C-V measurement of Pt/Ti/Pt/Au contact

Figure 4.5.2-7 shows the voltage dependence of junction capacitance. The positive shifts of the C-V curves after annealing were due to the changes of the Schottky barrier height and the effective Schottky barrier thickness which were caused by the Pt diffusion into the InAlP layer after annealed at different annealing temperatures. No increase in the capacitance curve was observed after annealing at higher than 300°C for 30 minutes. This was due to the diffusion of Pt into InAlP layer which also caused the positive shift of the I-V curve. The increase in the capacitance after annealed at 300°C can be explained by the existence of donor type surface trap, which situated at the deep level of InAlP and serve as parasitic components for the schottky capacitance. A large trap density also led to an increase in the measured capacitance at low frequency. The increase in capacitance after thermal treatment reflected the increase of the defects and the surface traps at the Pt/InAlP interface.

4.5.2-c Sheet resistance of Pt/Ti/Pt/Au on InAlP
The sheet resistances of these structures were shown in Figure 4.5.2-8. It was found that the sheet resistance of the film increased with increasing temperature. The sheet resistance slowly increased to 24.3 $\text{m} \Omega/\square$ after 300$^\circ\text{C}$ annealing for 30 minutes, and then increased sharply after 400$^\circ\text{C}$ annealing for 30 min. Therefore, it seems that the enlargement of Pt grains and the annihilation of defects were most likely the cause of the slow increase in the sheet resistance. The sharp change in the sheet resistance after 400$^\circ\text{C}$ for 30 minutes was mainly due to the formation of the intermetallic compounds or the defects between Pt and InAlP layer.

4.5.2-d TEM Image of Pt/Ti/Pt/Au sample after thermal annealing

Figure 4.5.2-9 shows a TEM image of the Pt/Ti/Pt/Au contact on InAlP epi structure after annealing at 400$^\circ\text{C}$ for 30 minutes. The EDX spectrums of EDX analysis 1.2.3 in Figure 4.5.2-9 are shown in Figure 4.5.2-10~4.5.2-12. The depth analysis confirms that Pt sinking into the InAlP layer and into the InGaAs channel while there are no traces of Ti and Au signals. These results substantiate that gate metal sinking in InAlP PHEMTs is initiated by the Pt inter-diffusion into the InAlP schottky layer and into the InGaAs channel. Figure 4.5.2-13 shows the interface between Pt and InAlP layer, the boundary due to Pt inter-diffusion into InAlP layer is not uniform. The interface reaction between Pt and InAlP TEM image is enlarged in Figure 4.5.2-14. The interface between Pt and InAlP was mixed up. It was found that Pt sunk into the InAlP layer after annealing.

4.5.3 The W/Ti/Pt/Au/InAlP Schottky Metal Structures
4.5.3-a Interfacial properties of W/Ti/Pt/Au schottky contact

The interfacial structure was investigated by XRD. Figure 4.5.3-1 shows XRD results of the W schottky contact samples before and after annealing at 200°C. W (200) (211) peaks were observed. The XRD showed no further peaks and the peaks of W became narrow after annealing at 200°C. It shows that W film becomes crystallized after annealing.

4.5.3-b Characteristics of W/Ti/Pt/Au schottky contact

The current-voltage (I-V) characteristics of the diodes after thermal annealing were shown in Figure 4.5.3-2. For annealing at 200°C for 30 minutes, the leakage current increased, however, after annealing at 300°C for 30 minutes, the leakage current remained the same up to 500°C. No positive shift of I-V curve was found after annealing up to 500°C for 30 minutes. It shows that W is a high thermal stability schottky barrier material on InAlP PHEMTs. Figure 4.5.3-3 showed the forward current for W/Ti/Pt/Au contact after annealed at different temperature. A decrease in forward current was obtained after annealed at higher temperature. This characteristic may be due to the increase of schottky barrier height with higher annealing temperatures. Figure 4.5.3-4, Figure 4.5.3-5 show the ideality factor and schottky barrier height of W/Ti/Pt/Au contact annealed at different temperatures. The Schottky barrier heights estimated by the measured I-V curve of the diodes were 0.63 eV, 0.67 eV, 0.72 eV, 0.75 eV and 0.78 eV, the estimated ideality factor were 1.65, 1.49, 1.42, 1.37 and 1.59 for as-deposited, 200°C, 300°C, and 400°C, 500°C samples.
respectively. The increase of schottky barrier height may be due to the intimate contact between W and InAlP layer. The breakdown voltage was defined as the applied voltage when leakage current is 0.002A. Figure 4.5.3-6 shows the reverse breakdown voltage of W/Ti/Pt/Au contact at different annealing temperature. The measured breakdown voltages were 13.6V, 15.6V, 15.3V, 16V and 17.5V, for as-deposited, 200°C, 300°C, 400°C and 500°C respectively. The reverse breakdown voltage for W/Ti/Pt/Au increases with annealing temperatures, this may be due to the increase in schottky barrier height or the intimate contact between InAlP and W.

4.5.3-c C-V measurement of W/Ti/Pt/Au contact

The Schottky diode samples with a diameter of 0.05 mm were annealed at different temperatures for C-V measurement. Figure 4.5.3-7 shows the voltage dependence of junction capacitance. The positive shifts of the C-V curves after annealing were due to the changes of the Schottky barrier height and the effective Schottky barrier thickness. There was still an increase in the capacitance curve after annealed at 500°C for 30 minutes. We suggest that the diode characteristics of the W/Ti/Pt/Au/InAlP diode are stable up to 500°C annealing.

4.5.3-d Sheet resistance of W/Ti/Pt/Au on InAlP

The sheet resistances of these structures were shown in Figure 4.5.3-8. It was found that the sheet resistance of the film increased with increasing
temperature. The sheet resistance of W/Ti/Pt/Au is much higher than Ti/Pt/Au contact and Pt/Ti/Pt/Au contact. The high sheet resistance is due to the low conductivity of W film. The sheet resistance slowly increased from 145.6 m$\Omega$/□ to 157.6 m$\Omega$/□ for as deposite and after 300°C annealing for 30 minutes samples, and then increased sharply after 400°C annealing for 30 minutes. It seems that the increase of defect density was the most likely cause for the increase of the sheet resistance.

4.6 DC Characteristics of the D-mode and E-mode InAlP PHEMTs with Ti/Pt/Au Gate

The I-V characteristics of the InAlP/InGaAs PHEMT are shown in Figure 4.6.1. The structure with 40$\mu$m gate-width and 0.4$\mu$m gate exhibit good pinch-off voltage of –0.5V and the saturation drain current ($I_{DSS}$) is 67mA/mm. The maximum current is 241mA/mm when $V_{gs}$ is 1V. The transconductance of the device at 1.5V drain-to-source voltage ($V_{ds}$) bias is shown in the Figure 4.6.2. The maximum transconductance is 302mS/mm. The pinch off voltage of the PHEMT is about -0.5V and from Figure 4.6.3, the breakdown voltage is -11V.

The I-V characteristic of the E-mode InAlP/InGaAs PHEMT was shown in Figure 4.6.4. The device with 125$\mu$m gate-width and 0.5$\mu$m gate has maximum current of 183mA/mm when $V_g$ at 2.5V. The threshold voltage is 209mV. The transconductance of the device at 1.5V drain-to-source voltage ($V_{ds}$) bias is shown in Figure 4.6.5. The maximum transconductance is 206 mS/mm. Figure 4.6.6 shows the schottky diode characteristics of the InAlP/InGaAs PHEMTs. The breakdown voltage is -14V and the turn on
voltage is 1.35V.

4.7 Effect of gate orientation on InAlP/InGaAs PHEMT characteristics

The DC characteristics of the InAlP PHEMTs with different gate orientations are shown in Figure 4.8.1 and Figure 4.8.2. The threshold voltage was measured from the extrapolation of the Ids versus Vgs curve. The threshold voltage was -33mV with gate along [0-1-1] direction and 32mV with gate along [0-11] direction. The Imax and Gm performances are better for devices with gate along [0-1-1] direction. The differences may be due to the orientation dependence of the electron distribution, electron mobility and the gate recess profile.

4.8 Performance comparison of InAlP/InGaAs PHEMTs with Ti/Pt/Au, Pt/Ti/Pt/Au and W/Ti/Pt/Au schottky metal contacts under thermal treatments.

4.8.1 Performance of InAlP/InGaAs PHEMTs with Ti/Pt/Au contact

Before annealing, the device exhibits a threshold voltage of -0.5 V and a maximum transconductance of 128.9 mS/mm. Figure 4.7.1 shows the transfer characteristics of a typical 0.6um gate length device before and after gate annealing. Following the measurement, the devices were annealed in a furnace at 250°C for 30 minutes and 3 hours, respectively. Afterannealing, the transfer curve was again measured. After annealing for 30 minutes, the threshold voltage of the device was shifted to -0.3V. In addition, the Gm was increased to 130 mS/mm. The increasing of Gm was
due to the Ti diffusion into the InAlP layer which reduced the distance between the gate metal front and the channel. After annealing for 3 hours, the threshold voltage shifted positively to -0.2V and the Gm decreased to 124mS/mm. The diffusion of Ti resulted in the decrease of Gm and the positive shift of threshold voltage. Schottky barrier heights and ideality factors were also measured and are shown in Table 4.1. The decrease of the schottky barrier height and increase of the ideality factor may be due to the inter-diffusion of Ti into the InAlP layer. The small decrease of schottky barrier height and the decrease of gate to channel spacing resulted in the positive shift of the threshold voltage.

4.8.2 Performance of InAlP/InGaAs PHEMTs with Pt/Ti/Pt/Au contact

Before annealing, the devices exhibit a threshold voltage of -0.2 V and a maximum transconductance of 139 mS/mm. Figure 4.7.2 shows the transfer characteristics of a typical 0.6um gate length device prior to annealing and after annealing. Following the measurements, the devices were annealed in furnace at 250°C for 30 minutes and 3 hours. After annealing for 30 minutes, the device has a threshold voltage of 0.1 V. In addition, the Gm increased to 164 mS/mm. However, the Gm decreased to 104 mS/mm after annealing for 3 hours. Schottky barrier heights, ideality factors and gate leakage currents were also measured and are shown in Table 4.2. The schottky barrier height increased from 0.65 eV to 0.71 eV with the gate leakage current decreasing from -9.73 uA/mm to -1.7 uA/mm after annealing at 250°C for 30 minutes. The Schottky barrier height increased and the gate leakage current reduced after 250°C for 30min
annealing due to the proper metal diffusion. The increase in schottky barrier height and the decrease in gate-to-channel spacing resulted in the positive threshold voltage shift and the increase of the transconductance. From this study, Pt appears to be the best choice for use as a gate metal in E-mode PHEMT due to the improvement of schottky characteristic and the positive shift of threshold voltage after proper annealing conditions. However, the leakage current increased rapidly after annealing for 3 hours and the Gm decreased. The over-diffusion of Pt would degrade the performance of the device. The condition of the thermal treatment needs to be optimized to avoid drastic degradation in performance.

4.8.3 Performance of InAlP/InGaAs PHEMTs with W/Ti/Pt/Au contact

Prior to annealing, the devices exhibit a threshold voltage of -0.225 V and a maximum transconductance of 95 mS/mm. Figure 4.7.3 shows the transfer characteristics of a typical 0.6um gate length device prior to gate anneal and after gate anneal. Following the pre-annealed measurements, the devices were annealed in furnace at 250°C for 30 minutes. After annealing, the transfer curves were again measured. After annealing, the device exhibits a threshold voltage of -0.223V. In addition, the Gm increases to 105 mS/mm. Schottky barrier heights, ideality factor and gate leakage currents were also measured and are shown in Table 4.3. The schottky barrier height increased from 0.67 eV to 0.69 eV with the gate leakage current increasing from -356 uA/mm to -358 uA/mm. It shows no further shift of threshold voltage and changes of schottky barrier heights and leakage currents. It reflects that the performance of devices with
W/Ti/Pt/Au schottky contact remains stable after thermal annealing at 250 °C for 30 minutes.