Chapter 2
Study of Schottky Contacts on InAlP

The ternary compound InAlP is a wide-bandgap semiconductor material. The high band gap and large delta Ec provide high electron mobility and high breakdown voltage, high schottky barrier height and low leakage current. InAlP layer also provides high etching selectivity during gate recess process. However, it is evident that although relatively high barrier is achievable for InAlP, there may be disparity between the measured results. The measured barrier height depends on the characterization techniques used, the InAlP epitaxial grown and the quality of the semiconductor surface, and the contact metal used.

2.1 Theory of Schottky Contacts[2.1]

When metal is making intimate contact with a semiconductor, the Fermi levels in the two material must be coincident at thermal equilibrium as shown in Figure 2.1. This can be achieved through a charge flow from semiconductor to metal. Thus a barrier forms at the interface and an equal and opposite space charge is contributed over the barrier region near the semiconductor surface.

A metal-semiconductor junction under forward and reverse bias is illustrated with Figure 2.2(a) and 2.2(b). As a positive bias is applied to the metal in Figure 2.2(a), the Fermi energy of the metal is lowered with respect to the Fermi energy in the semiconductor. This results in a smaller potential drop across the semiconductor. The balance between diffusion and
drift is disturbed and more electrons will diffuse towards the metal than the
number drifting into the semiconductor. This leads to a positive current
through the junction at a voltage comparable to the built-in potential.

As a negative voltage is applied shown in Figure 2.2(b), the Fermi
energy of the metal is raised with respect to the Fermi energy in the
semiconductor. The potential across the semiconductor now increases,
yielding a larger depletion region and a larger electric field at the interface.
The barrier, which restricts the electrons to the metal, is unchanged so that
that barrier, independent of the applied voltage, limits the flow of electrons.
The metal-semiconductor junction with positive barrier height has therefore
a pronounced rectifying behavior. A large current exists under forward bias,
while almost no current exists under reverse bias.

When a metal is placed in intimate contact with a wide-band-gap
semiconductor of moderate doping the resulting junction is a diode. The
thermionic emission theory assumes that electrons, with an energy larger
than the top of the barrier, will cross the barrier provided they move
towards the barrier. The actual shape of the barrier is hereby ignored. The
current density in the forward direction may be express as

\[ J = A^* T^2 \exp \left( -\frac{q\phi_b}{kT} \right) \exp \left( \frac{qV}{nkT} \right), \text{ for } V > \frac{KT}{q} \]

\[ = J_S \exp \left( \frac{qV}{nkT} \right) \]

\[ J_S = A^{**} T^2 \exp \left( -\frac{q\phi_b}{kT} \right) \]

\[ A^{**} = \frac{4\pi q m^* k^2}{h^3} \]
where $J$ is the current density, $A^{**}$ is the effective Richardson Constant, $m^*$ is 0.22 for AlInP, $T$ is the absolute temperature, $q$ is the electron charge, $\varphi_b$ is the barrier height, $k$ is Boltzmann constant, $V$ is the applied voltage, and $n$ is the ideality factor. The ideality factor would be 1 for a perfect Schottky diode. In practice, $n$ is generally between 1.0 and 2, with the value increasing with increasing doping in the semiconductor. From the y-axis intercept and the slope of the $\ln J$ vs $V$ plot at the forward bias, the values of the $\varphi_b$ and $n$ can be determined.

There are four methods used to measure the barrier height of metal-semiconductor junctions: current-voltage, capacitance-voltage, activation energy, and photoelectric methods. The first two methods are the simplest for general in-process characterization. For Current-voltage method,

$$\ln(J) = \ln(J_s) + \frac{qV}{nkT}, \text{ for } V > kT/q$$

where

$$J_s = A^{**}T^2 \exp(-\frac{q\varphi_b}{KT})$$

Therefore, a plot of $\ln J$ as a function of $V$ should result in a straight line having slope $q/nkT$ and Y axis intercept $\ln J_s$. Note that for sufficiently small and sufficiently large currents, the linear relationship between $\ln J$ and $V$ does not hold, but is generally quite accurate over many orders of magnitude of current. Measurement of the slope allows calculation of the ideality factor, $n$:

$$\text{Slope} = \frac{q}{nkT}, \quad n = \frac{q}{\text{slope} \cdot kT}$$

If we know the value of $J_s$ (from the intercept point), the barrier height may be calculated as follows:
\( \phi_b = (kT/q) \ln(A^{**T^2}/J_s) \)

For actual devices such as FETs, the gate length may be so small that gate area is difficult to measure accurately. However, because both these terms appear inside the logarithm, the barrier height \( \phi_b \) is relatively insensitive to errors in those terms.

The reverse breakdown voltage is an important parameter of many schottky barrier devices. The most important mechanism in junction breakdown is avalanche multiplication (or impact ionization). As the electric field in the semiconductor increase, the carriers gain sufficient energy to create electron-hole pairs by impact ionization. These carriers also gain energy in the field, and create more electron-hole pairs. The process can avalanche, leading to breakdown and large current flow. Because breakdown is intimately related to the electric field, geometrical effects that affect the electric field configuration will also affect breakdown voltage.

Breakdown voltages on actual devices are also affected by other considerations, such as surface effects. These make the breakdown voltage of actual devices sensitive to the process details. Any phenomenon that affects the surface between the gate and the ohmic contact is a possible cause of the variation of breakdown voltages also. It seems that minor surface effects could modify the electric field configuration near the gate edge, thereby change the breakdown voltage.

We can obtain the capacitance as a function of the applied voltage by taking the derivative of the charge with respect to the applied voltage yielding:
The equation indicates that the expression of a parallel plate capacitor still applies. One can understand this once realizing that the charge added/removed from the depletion layer is only at the edge of the depletion region. While the parallel plate capacitor expression seems to imply that the capacitance is constant, the metal-semiconductor junction capacitance is not constant since the depletion layer width, $x_{d}$, varies with the applied voltage.

2.2 Interfacial Reaction between Semiconductor and Schottky metal

The metal-semiconductor interface behavior has attracted a great deal of attention because of the contact problem in the microelectronic device. Many investigations have been carried out in order to understand the microstructure and kinetics of metal-semiconductor interfacial reactions, and the related electrical properties and electronics structures. In comparison, it appears that much less has been studied about the interfacial contact reaction between metal and InAlP.

Since the electrical properties, such as the barrier height and the contact resistance, of metal-semiconductor junctions are generally sensitive to the formation of any intermetallics, a preferred, through not sufficient condition for a high reliability of GaAs devices utilizing schottky barriers is that the metal-semiconductor contact be metallurgically nonreactive [2.2].

Metallization is a fundamental aspect to the fabrication of both ohmic and schottky contacts. Primary considerations in the choice of a contact metal are: the desired electrical properties, good adhesion to the
semiconductor, chemical resistance, thermal stability, and good morphology. The electrical and thermal stabilities of metal/GaAs interfaces impact on many technical areas of GaAs devices. The schottky barrier height of the schottky contact is one of the most important parameters of the devices. A high barrier height improves the transconductance and breakdown voltage of the electronic devices, leading to the enhancement of the power performance. The Pt/Au and Ti/Pt/Au schottky metals are the most important multilayer metallization systems, and have been widely used in the fabrication of schottky barrier diodes, MESFETs and HEMTs [2.3]. The schottky characteristics were analyzed utilizing thermionic-emission theory, where the saturation current, barrier height, and ideality factor n were determined from the relationship between the current density and the applied voltage. The schottky contacts are usually deposited after ohmic contact fabrication, but they must be resistive to other thermal shocks during fabrication processes and practical applications. In this study, metal/semiconductor schottky structures, Au/Pt/Ti on InAlP, Au/Pt/Ti/Pt on InAlP and Au/Pt/Ti/W on InAlP were formed, and the thermal stability and I-V characteristics of the structures were investigated. Schottky parameters (ideality factor, schottky barrier height, reverse leakage current, and reverse breakdown voltage) were compared and analyzed to evaluate the stability of each schottky contact structure under study.

In a schottky metal structure, gold provides low resistance electrical paths, the platinum acts as the diffusion barrier between the gold and the titanium layer, and the titanium provides a stable schottky barrier and a strong bond to the GaAs. Gold can’t be placed directly on GaAs because it
does not adhere strongly and it forms an eutectic that has poor electrical properties. However, titanium forms a good bond to GaAs and titanium-to-GaAs schottky diodes still have a barrier height of about 0.8 eV after a 30 min anneal at 480°C [2.4]. A metallization consisting of gold on top of titanium directly would not work because gold diffuses at a rate of 0.2 nm per hour into titanium at 300°C [2.5]. The combination of titanium, platinum and gold gives good adhesion, a stable schottky barrier height, high resistance to interdiffusion, and good electrical conduction. In addition, it has been reported that the characteristics of Ti/Pt/Au on GaAs Schottky diodes changed from those expected for titanium-to-GaAs barriers to those expected for platinum-to-GaAs barriers after the diodes were annealed at 500°C for 2 hrs [2.6].

2.3 Use Pt as schottky contact metal for E-mode device fabrication

Pt is one of the metals with large function of 5.7 eV, whereas that of the widely used Ti schottky contact metal, the work function is 4.3eV. Moreover, Pt easily diffuses into III-V semiconductor materials, and forms stable compound with group V materials [2.7][2.8], which has higher work function than before diffusion. The amount of the gate sinking depth caused by Pt diffusion can be controlled by using Pt/Ti/Pt/Au gate contact structure with sufficient thin bottom Pt layer. The schottky barrier height of Pt/InGaP/InAlAs diodes was about 0.7eV, where that of Ti/InGaP/InAlAs diodes was 0.59eV. Thus a relatively high schottky barrier was obtained by using Pt as the contact layer [2.9]. Although, the Pt exhibited a high Schottky barrier height which can reduce the gate leakage current, there were few reports investigating Pt and InAlP interfacial reactions. The
Pt/InP and Pt/GaAs interfacial reactions had been reported. After thermal annealing, both Pt-In phase and PtP$_2$ were presented at the Pt and InP interface [2.10]. In addition, the PtGa and PtAs$_2$ were also observed after the Pt and GaAs interfacial reaction [2.11]. In this study, the material analysis and current-voltage characterization were carried out to investigate the interfacial reactions between Pt and InAlP Schottky barrier layer, and the performances of the Pt/InAlP Schottky contact devices.

Since the electrical properties, such as the barrier height and the contact resistance of the metal-semiconductor junctions are generally sensitive to the formation of any intermetallics, though not sufficient condition for a high reliability of GaAs devices utilizing Schottky barriers is that the metal-semiconductor contact be metallurgically nonreactive. Electrical studies of W/n-GaAs Schottky diodes have shown that aging at 350 to 500°C does not significantly change the forward I-V characteristics of the diodes, and this reflects a high degree of thermal stability of the W/GaAs Schottky structure. The present results suggest that a W film may act as a good barrier to the outdiffusion of Ga [2.2].

Gate-metal diffusion has been observed in field-effect transistors, such as GaAs metal-semiconductor FETs, GaAs/InGaAs/GaAs pseudomorphic high electron mobility transistors (HEMTs), and InAlAs/InGaAs/InP HEMTs. Gate metal diffusion which occurs during the fabrication process and also during the device operation is very important since gate diffusion can affect the uniformity and the reliability of the devices through changes in the device parameters, such as threshold voltage, transconductance, and the gate capacitance. Metal diffusion in a semiconductor has been investigated using
spectroscopic methods, such as Rutherford back-scattering spectroscopy, Auger electron spectroscopy, and X-ray photoelectron spectroscopy. However, these methods do not provide nanometer-scale resolution that is required in the investigation of gate metal diffusion in complex heterostructure FET structures typically consisting of several thin epi layers. Transmission electron microscopy (TEM) analysis has been utilized for studying the gate metal diffusion since it enables atomic-scale depth profiling of elements. Even though TEM analysis provides nano-scale resolution, TEM itself does not provide the information on the effects of the metal diffusion on the electrical properties of devices. Therefore, to obtain a complete picture of device-related issues, it is desirable to couple the TEM method and electrical measurements. Capacitance-voltage (C-V) measurement has been utilized to investigate two-dimension electron gas properties of the HEMT structures. C-V measurement can also reveal carrier distribution as well as device parameters, such as gate capacitance and turn-on voltage. The C-V characteristic is very sensitive to the diffusion depth since diffused metal reduces the effective thickness of the schottky barrier layer [2.12].

The threshold voltage of a conventional delta-doped HEMT can be obtained by solving Poisson’s equation in one dimension, and can be expressed as

\[ V_T = \phi_b - \frac{\Delta E_c}{q} \cdot \frac{qN_d d_d}{\varepsilon} \]

where

- \( \phi_b \) schottky barrier height of metal on the Schottky layer
- \( \Delta E_c \) conduction band discontinuity between the high bandgap schottky
layer and the low-bandgap channel;

\[ N_d \quad \text{delta-doping sheet concentration}; \]

\[ d \quad \text{distance between the gate and the doping plane}; \]

\[ \varepsilon \quad \text{permittivity of the Schottky layer.} \]

According to the equation, four parameters \( \phi_b, N_d, \varepsilon, d \) effect the threshold voltage: and since the gate annealing temperature is too low to cause significant modification of the semiconductor heterostructure, the \( \Delta E_c \) between InAlP and InGaAs must remain identical to the preannealed value. Similarly, there is no reason to believe that the annealing alters the doping concentration, As a result, two explanations are possible for the increase in the threshold voltage of the device, namely an increase in \( \phi_b \) and/or a decrease in \( d \). It reveals that \( \phi_b \) must be substantially large in order to achieve E-mode characteristic. Recently, Pt has attracted much attention as a gate contact metal for E-HEMT devices. A high doping concentration leads to good device characteristics such as high extrinsic transconductance, large current drive, and high speed operation, but the high charge density also requires a rather large negative gate potential to fully deplete the channel of the FET, making enhancement mode operation impossible. Likewise, a small gate-to-channel distance is desirable for a large extrinsic transconductance as well as a positive threshold voltage. However, as this distance is reduced, the reverse gate leakage increases rapidly, leading to a low breakdown voltage as well as poor pinch-off characteristics of the transistor. A compromise must be met between the sheet doping density and the gate-to-doping plane distance in order to fabricate E-mode devices [2.13]. In this study, a Pt/Ti/Pt/Au schotky
contact structure was used in E-mode device fabrication. Thermal annealing was applied to drive the gate metal front move into the semiconductor schottky layer and shorten the gate-to-channel distance, resulting in E-mode characteristic of the InAlP PHEMT.