AIP | Applied Physics Letters

Improved performance and reliability for metal-oxide-semiconductor field-effect-transistor with fluorinated silicate glass passivation layer

Chih-Ren Hsieh, Yung-Yu Chen, and Jen-Chung Lou

Citation: Applied Physics Letters **96**, 022905 (2010); doi: 10.1063/1.3279140
View online: http://dx.doi.org/10.1063/1.3279140
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/96/2?ver=pdfcov
Published by the AIP Publishing

Articles you may be interested in

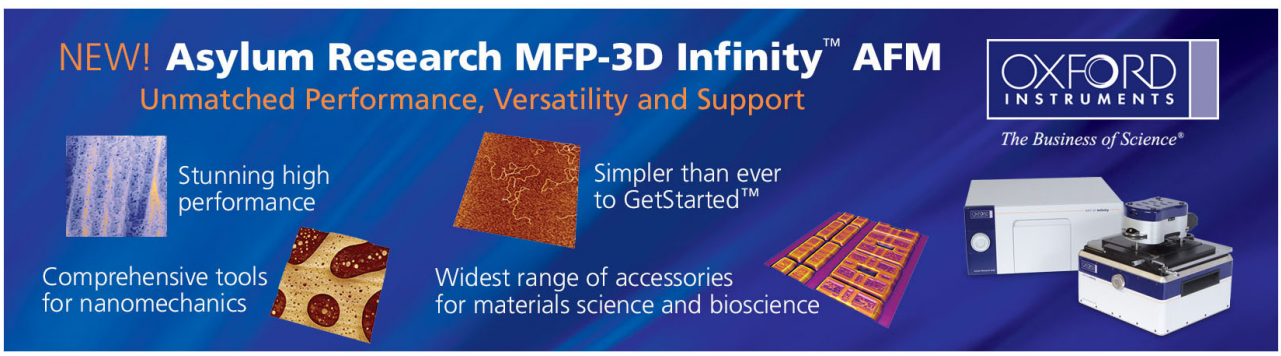
Fluorine passivation of vacancy defects in bulk germanium for Ge metal-oxide-semiconductor field-effect transistor application
Appl. Phys. Lett. **101**, 072104 (2012); 10.1063/1.4746389

Characterization of fast charge trapping in bias temperature instability in metal-oxide-semiconductor field effect transistor with high dielectric constant
Appl. Phys. Lett. **96**, 142110 (2010); 10.1063/1.3384999

Enhancement mode GaAs metal-oxide-semiconductor field-effect-transistor integrated with thin AlN surface passivation layer and silicon/phosphorus coimplanted source/drain
J. Vac. Sci. Technol. B **27**, 214 (2009); 10.1116/1.3025909

Effective surface passivation methodologies for high performance germanium metal oxide semiconductor field effect transistors
Appl. Phys. Lett. **93**, 192115 (2008); 10.1063/1.3028025

Fabrication of gate stack with high gate work function for implantless enhancement-mode GaAs n -channel metal-oxide-semiconductor field effect transistor applications
Appl. Phys. Lett. **92**, 123513 (2008); 10.1063/1.2905259



This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Wed, 30 Apr 2014 12:01:13

Improved performance and reliability for metal-oxide-semiconductor field-effect-transistor with fluorinated silicate glass passivation layer

Chih-Ren Hsieh,[1] Yung-Yu Chen,[2,a)] and Jen-Chung Lou[1]
[1]*Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan*
[2]*Department of Electronic Engineering, Lunghwa University of Science and Technology, Guishan, Taoyuan 333, Taiwan*

(Received 10 November 2009; accepted 5 December 2009; published online 13 January 2010)

The superior characteristics of the fluorinated HfO_2/SiON gate dielectric are investigated comprehensively. Fluorine is incorporated into the gate dielectric through fluorinated silicate glass (FSG) passivation layer to form fluorinated HfO_2/SiON dielectric. Fluorine incorporation has been proved to eliminate both bulk and interface trap densities due to Hf–F and Si–F bonds formation, which can strongly reduce trap generation as well as trap-assisted tunneling during subsequently constant voltage stress, and results in improved electrical characteristics and dielectric reliabilities. The results clearly indicate that the fluorinated HfO_2/SiON gate dielectric using FSG passivation layer becomes a feasible technology for future ultrathin gate dielectric applications. © *2010 American Institute of Physics*. [doi:10.1063/1.3279140]

High dielectric constant (high-κ) materials are introduced as the alternative gate dielectrics, since they can significantly suppress the intolerable leakage current present in the conventional ultrathin oxide (SiO_2).[1] Various high-κ dielectrics, including tantalum oxide (Ta_2O_5), yttrium oxide (Y_2O_3), zirconium oxide (ZrO_2), cerium oxide (CeO_2), strontium titanate ($SrTiO_3$), and hafnium oxide (HfO_2) have been extensively studied as the gate dielectric. Among these high-κ dielectrics, HfO_2 is the most potential candidate under investigation, due to the high dielectric constant (~25), wide band gap (~5.5 eV), high conduction band offset (~1.5 eV), and good thermal stability with silicon substrate.[2] However, unlike SiO_2 or oxynitride (SiON), directly deposited HfO_2 dielectric on the silicon substrate without interface treatment usually results in high defect densities and poor stress immunity.[3,4] Consequently, the bulk defects and interface trap densities may become the critical problem for future ultralarge scale integration (ULSI) technology applications of the HfO_2 gate dielectric, leading to significant threshold voltage (V_{TH}) shift and device performance degradation.

Recently, the dielectric properties and device characteristics for the fluorinated high-κ gate stacks have been studied comprehensively.[5–7] Fluorine incorporation within the high-κ films can recover interfacial dangling bonds and bulk oxygen vacancies during subsequent processes, which is useful to reduce gate leakage current[6,7] and improve dielectric reliabilities. Several fluorine passivation technologies have been mentioned to improve device reliabilities, such as tetrafluoromethane (CF_4) plasma treatment,[8] channel fluorine implantation,[9] source/drain region fluorine implantation,[10] and F_2 gas anneal.[11] In this letter, a fluorination process using fluorinated silicate glass (FSG) passivation layer has been introduced. The electrical characteristics and dielectric reliabilities of n-channel metal-oxide-semiconductor field-effect-transistors (nMOSFETs) with the FSG fluorinated HfO_2/SiON gate dielectric has been investigated comprehensively.

The nMOSFETs were fabricated on 6 in. p-type (100) Czochralski silicon wafer with 1–10 Ω cm resistivity utilizing a conventional self-aligned process, followed by the standard cleaning with a hydrofluoric acid last process. Prior to the HfO_2 gate dielectric deposition, less than 1 nm interfacial SiON was grown by rapid thermal processing in the nitrous oxide (N_2O) ambient at 800 °C for 30 s. The 4 nm HfO_2 gate dielectric was subsequently deposited by the AIXTRON metal organic chemical vapor deposition system at 500 °C, followed by postdeposition anneal at 600 °C in nitrogen (N_2) ambient for 30 s to improve HfO_2 film quality. A 200 nm poly-Si gate was then deposited by low-pressure chemical vapor deposition system using silane (SiH_4) gas at 620 °C.

After gate electrode patterning by I-line lithography stepper and subsequently phosphorous implantation at 25 keV, 5×10^{15} cm^{-2}, dopants were then activated at 950 °C for 30 s in N_2 ambient. Afterward, a 300 nm FSG passivation layer was deposited using the plasma-enhanced chemical vapor deposition (PECVD) system at 300 °C with SiH_4, N_2O, and CF_4. Undoped SiO_2 passivation layer was deposited at the SiH_4 and N_2O ambient for reference. To avoid fluorine diffusing out from the FSG layer during the following high temperature processes while improving the thermal stability of the FSG film, a 100 nm silicon nitride layer was deposited above the FSG film using PECVD system.[12] Finally, contact holes etching and Al metallization were performed using standard complementary metal-oxide-semiconductor process, followed by 400 °C sintering for 30 min in N_2 ambient.

The electrical properties and reliability characteristics of the HfO_2/SiON gate stacked nMOSFETs were measured using the Hewlett-Packard (HP) 4156C semiconductor parameter analyzer and HP81110A pulse generator. The capacitive effective thickness (CET) of the gate dielectric was extracted from the high-frequency (1 MHz) capacitance-voltage (*C-V*) curves at strong inversion without considering the quantum effect. Charge pumping current was measured with fixed am-

a)Electronic mail: yungyu@mail.lhu.edu.tw.

 © 2010 American Institute of Physics

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Wed, 30 Apr 2014 12:01:13

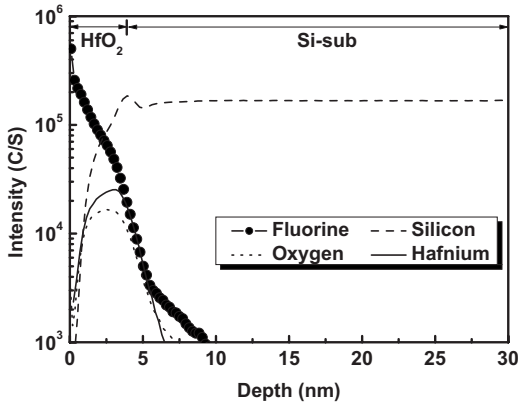


FIG. 1. SIMS depth profile of the FSG passivated $HfO_2/SiON$ gate dielectric.

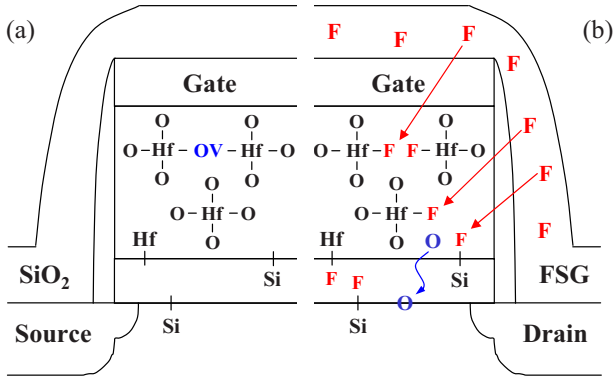


FIG. 3. (Color online) Schematic diagram for the nMOSFET with (a) SiO_2 and (b) FSG passivation layer. Oxygen vacancy is defined as OV in the figure.

plitude method at 1 MHz. Furthermore, the content and distribution of the fluorine atom was measured by secondary-ion mass spectroscopy (SIMS).

Figure 1 shows the SIMS depth profile of the FSG passivated $HfO_2/SiON$ gate dielectric. The experimental result clearly demonstrates FSG passivation layer is effective to incorporate fluorine into the $HfO_2/SiON$ gate stack, which can help to terminate the oxygen vacancies to form Hf–F bonds. From SIMS analyses, fluorine atoms can further diffuse into the Si channel, which also has a high probability to passivate interface dangling bonds to form Si–F bonds. Moreover, fluorine atoms diffused from the FSG layer are likely to assemble at the top interface between $HfO_2/SiON$ dielectric and poly-Si gate. The high frequency *C-V* characteristics for the $HfO_2/SiON$ gate stack with FSG and SiO_2 passivation layer are indicated in Fig. 2. The extracted CET is 3.83 and 4.21 nm for the nMOSFETs with SiO_2 and FSG passivation layer, respectively. Since fluorine atom has the highest electronegativity, the doped fluorine atoms from the FSG layer exhibit high potential to substitute the oxygen atoms, then replaces the Hf–O bonds by the Hf–F bonds. Part of the residual oxygen may diffuse toward the interface between $HfO_2/SiON$ dielectric and underneath silicon substrate, then react with the silicon dangling bonds at the interface to growth low dielectric constant interfacial layer.[13] The measured capacitance is therefore reduced, and results in increased CET. The mechanism of the interfacial reoxidation is also shown in Fig. 3.

Figure 4 compares the electron mobility extracted from split *C-V* method for the nMOSFETs with FSG and SiO_2 passivation layer. Replacing conventional SiO_2 passivation layer by the FSG passivation layer, larger than 7% and 49% improvement is observed for peak (~0.25 MV/cm) and high field (0.8 MV/cm) mobility, respectively. Since fluorine incorporation can be used to passivate both the bulk oxygen vacancies and interface dangling bonds through Hf–F and Si–F bonds formation, which is also plotted in Fig. 3, the nMOSFET with fluorinated $HfO_2/SiON$ gate dielectric is expected to suppress the charge trapping and less interfacial charge scattering.[5] Higher electron mobility as well as higher saturation drain current (not shown) are therefore obtained using FSG passivation layer instead of SiO_2 passivation layer.

Figure 5 shows the Weibull plot of charge-to-breakdown (Q_{BD}) distribution for nMOSFETs with FSG and SiO_2 passivation layer at 5.9 V constant voltage stress. The 63% failure rate Q_{BD} is 45.6 and 132 C/cm^2 for the $HfO_2/SiON$ gate dielectric with SiO_2 and FSG passivation layer, respectively. Larger than 2.5 times breakdown charges improvement can be obtained using FSG fluorine incorporation process. Since the slope of the Weibull distribution is an important factor in reliability calculation to extrapolate lifespan to different percentiles, the Weibull slope (β) of the Q_{BD} distribution is further extracted to examine the dielectric reliability. The extracted Weibull slope of the Q_{BD} distribution can be also improved from 5.6 to 8.4 by replacing SiO_2 passivation layer with FSG passivation layer. Consequently, the optimized flu-

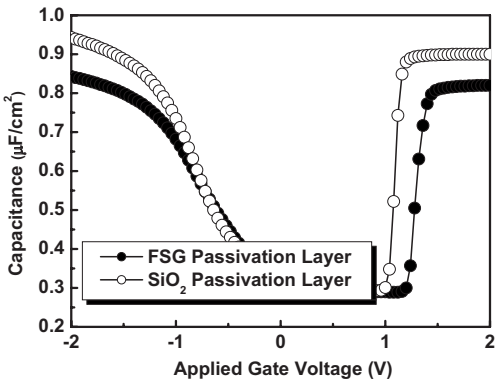


FIG. 2. High frequency *C-V* curve for the $HfO_2/SiON$ gate stack with FSG and SiO_2 passivation layer.

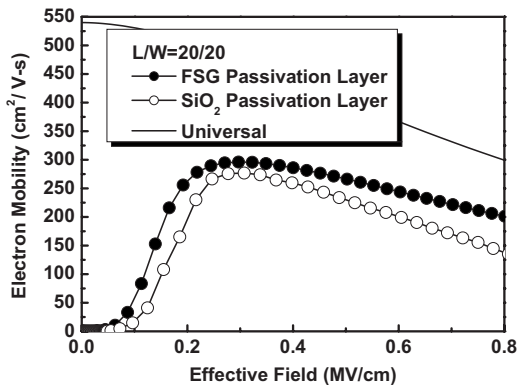


FIG. 4. Electron mobility extracted by spilt *C-V* method for nMOSFETs with FSG and SiO_2 passivation layer.

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Wed, 30 Apr 2014 12:01:13

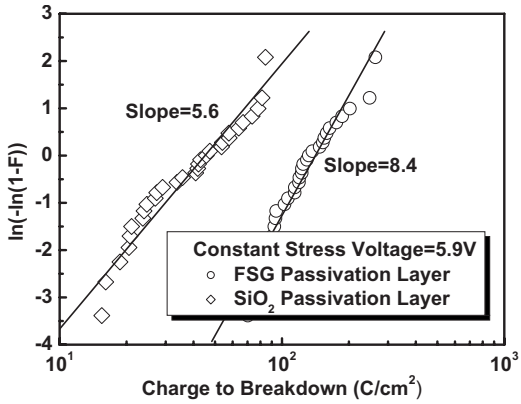


FIG. 5. Weibull plot of charge-to-breakdown distribution for nMOSFETs with FSG and SiO_2 passivation layer at 5.9 V constant voltage stress.

orinated $HfO_2/SiON$ gate dielectric not only improves the Q_{BD} but also narrows the Q_{BD} distribution, which can be mainly ascribed to diminish the dangling bonds and oxygen vacancies with fluorine atoms, consistent with previous results.

Figure 6 presents the stress-induced bulk trap generation (ΔN_{ot}) and interface trap generation (ΔN_{it}) for nMOSFETs with FSG and SiO_2 passivation layer. The ΔN_{ot} was extracted from threshold voltage shift during constant current stress, while ΔN_{it} was extracted from charge pumping current increment. After constant voltage stressing, both bulk trap and interface trap generation are decreased while introducing FSG fluorination process, which can be ascribed to the robust Hf–F and Si–F bonds located at the dielectric bulk and interface, respectively, which was also indicated in Fig. 3. Besides, constant voltage stress induced dielectric degradation is likely to occur within the $HfO_2/SiON$ bulk dielectric, rather than occur at the interface between $HfO_2/SiON$ dielectric and silicon substrate. Since the threshold voltage shift is mostly related with the bulk traps rather than the

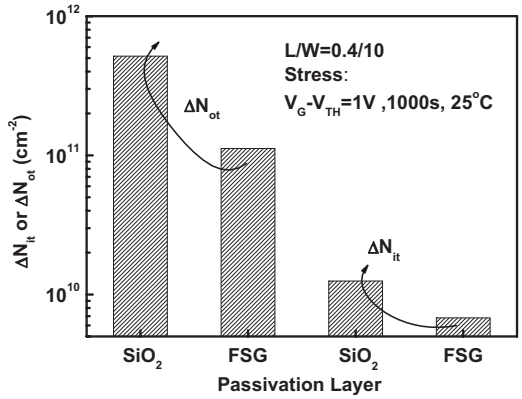


FIG. 6. Stress-induced bulk trap generation (ΔN_{ot}) and interface state generation (ΔN_{it}) for nMOSFETs with FSG and SiO_2 passivation layer at $V_G - V_{TH} = 1$ V constant voltage stress.

interface traps,[14] the result clearly concludes that the fluorinated $HfO_2/SiON$ dielectric exhibits a bulk dominant degradation characteristic, and the FSG fluorination process is more effective to passivate interface defects (Si–F bonds formation) than to passivate bulk defects (Hf–F bonds formation) to resist subsequent constant voltage stress.

As a conclusion, characteristics of the fluorinated $HfO_2/SiON$ gate dielectric are studied thoroughly. FSG passivation layer is effective to incorporate fluorine atoms located at both the $HfO_2/SiON$ dielectric bulk and the interface. The incorporated fluorine atoms within the dielectric bulk have a high tendency to passivate either oxygen vacancies or silicon dangling bonds, then form strong binding energy Hf–F and Si–F bonds within the dielectric bulk and the interface, respectively. Trap-assisted tunneling as well as trap generation during subsequently constant voltage stress can be drastically suppressed, and superior electrical characteristics and dielectric reliabilities have been therefore demonstrated. Moreover, FSG fluorination process has been proved to effectively passivate interface defects than to passivate bulk defects to resist subsequent constant voltage stress. The results clearly indicate that the fluorinated $HfO_2/SiON$ gate dielectric using FSG passivation layer possesses high potential to be integrated with currently ultrathin gate dielectric applications.

[1]G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys. **89**, 5243 (2001).
[2]L. Kang, Y. Jeon, K. Onishi, B. H. Lee, W.-J. Qi, R. Nieh, S. Gopalan, and J. C. Lee, Tech. Dig. VLSI Symp. **2000**, 44.
[3]Y. Kim, G. Gebara, M. Freiler, J. Barnett, D. Riley, J. Chen, K. Torres, J. Lim, B. Foran, F. Shaapur, A. Agarwal, P. Lysaght, G. Brown, C. Young, S. Borthakur, H. Li, B. Nguyen, P. Zeitzoff, G. Bersuker, D. Derro, R. Bergmann, R. Murto, A. Hou, H. Huff, E. Shero, C. Pomarede, M. Givens, M. Mazanec, and C. Werkhoven, Tech. Dig. - Int. Electron Devices Meet. **2001**, 455.
[4]S. Guha, E. P. Gusev, H. Okorn-Schmidt, M. Copel, L.-Å. Ragnarsson, and N. A. Bojarczuk, Appl. Phys. Lett. **81**, 2956 (2002).
[5]H.-H. Tseng, P. J. Tobin, S. Kalpat, J. K. Schaeffer, M. E. Ramon, L. R. C. Fonseca, Z. X. Jiang, R. I. Hegde, D. H. Triyoso, and S. Semavedam, IEEE Trans. Electron Devices **54**, 3267 (2007).
[6]H.-S. Jung, S. K. Han, H. Lim, Y.-S. Kim, M. J. Kim, M. Y. Yu, C.-K. Lee, M. S. Lee, Y.-S. You, Y. Chung, S. Kim, H. S. Baik, J.-H. Lee, N.-I. Lee, and H.-K. Kang, Tech. Dig. VLSI Symp. **2006**, 162.
[7]M. Inoue, S. Tsujikawa, M. Mizutani, K. Nomura, T. Hayashi, K. Shiga, J. Yugami, J. Tsuchimoto, Y. Ohno, and M. Yoneda, Tech. Dig. - Int. Electron Devices Meet. **2005**, 413.
[8]W.-C. Wu, C.-S. Lai, S.-C. Lee, M.-W. Ma, T.-S. Chao, J.-C. Wang, C.-W. Hsu, P.-C. Chou, J.-H. Chen, K.-H. Kao, W.-C. Lo, T.-Y. Lu, L.-L. Tay, and N. Rowell, Tech. Dig. - Int. Electron Devices Meet. **2008**, 1.
[9]W. C. Wu, C.-S. Lai, T.-M. Wang, J.-C. Wang, C. W. Hsu, M. W. Ma, W.-C. Lo, and T. S. Chao, IEEE Trans. Electron Devices **55**, 1639 (2008).
[10]Wen-Tai Lu, C.-H. Chien, W.-T. Lan, T.-C. Lee, P. Lehnen, and T.-Y. Huang, IEEE Electron Device Lett. **27**, 240 (2006).
[11]M. Chang, M. Jo, H. Park, H. Hwang, B. H. Lee, and R. Choi, IEEE Electron Device Lett. **28**, 21 (2007).
[12]P. F. Chou and Y. L. Cheng, Tech. Dig. VLSI Symp. **2001**, 257.
[13]Y. Yasuda and C. Hu, Tech. Dig. - Int. Electron Devices Meet. **2006**, 1.
[14]C. S. Lai, W. C. Wu, J. C. Wang, and T. S. Chao, Appl. Phys. Lett. **86**, 222905 (2005).

This article is copyrighted as indicated in the article. Reuse of AIP content is subject to the terms at: http://scitation.aip.org/termsconditions. Downloaded to IP: 140.113.38.11 On: Wed, 30 Apr 2014 12:01:13