Chapter 5

Conclusions and Future Works

In this thesis, we propose a 3D IC placement with thermal considerations. We first performed a 3D IC partition with a two-layer FM partition together with a multi-layer FM partition. We then performed a thermal-aware 3D IC placement by partitioning-based placement and simulated annealing refinement. In partitioning-based placement, we use net-weighting and white-space distribution to consider heat dissipation. We obtained trade-off among temperature, wirelength, and via costs. The experimental results show the algorithm can obtain a reduction in the temperature with little wirelength increase.

For the future work on thermal placement, the power analysis should be more accurate, which have heavy impact on heat dissipation. Thermal via insertion would be a good method to solve 3D thermal problem and many works have already focus on it. Therefore, considering thermal via during 3D IC placement would be a task to work on.

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