An Efficient Semi-Empirical Model of the $I-V$ Characteristics for LDD MOSFET's

STEVE SHAO-SHIUN CHUNG, MEMBER, IEEE, TZANG-SI LIN, AND YUH-GONG CHEN

Abstract—This paper describes a unified and computationally efficient SPICE model for accurate prediction of the $I-V$ characteristics of small-geometry lightly doped drain (LDD) MOSFET's. It was developed based on the enhancement of the SPICE LEVEL3 MOS model and a novel parameter extraction method. It supports the design of both short-channel and narrow-gate-width LDD MOSFET's with any kind of channel or field implant. Particularly, a new semi-empirical approach to model the threshold voltage of LDD MOSFET's is demonstrated for the first time, in which small geometry effect is implemented. The model is applicable to LDD MOSFET's with effective channel lengths and channel widths down to the submicrometer range and nonuniformly doped substrate. These two resistors account for the drain-to-source series resistance effect and are functions of drain-source voltage in the linear device operating region. All of the modeled parameters are taken from the experimentally measured $I-V$ characteristics and preserve physical meaning. In addition, automatic extraction of device parameters for SPICE built-in LDD MOSFET models has also been developed. Comparisons between the measured and modeled threshold voltages and $I-V$ characteristics show excellent agreement for a wide range of channel lengths, widths, and biases, which fully supports the accuracy of the model and makes it suitable for computer-aided design of integrated circuits.

NOMENCLATURE

- $a$: Body-effect charge sharing factor.
- $C_{ox}$: Oxide capacitance per unit area.
- $\delta L$: Reducing length due to channel length modulation.
- $\Delta L$: Channel length reduction.
- $\Delta W$: Channel width reduction due to bird's beak and field implant.
- $E_c$: Critical field (in volts per centimeter).
- $\epsilon_s$: Dielectric constant of the silicon.
- $I_D$: Drain current (in amperes).
- $I_{DSAT}$: Saturation current at the onset of the saturation region.
- $I_{DSS}$: Drain current in the saturation region.
- $K(L, V_{GS})$: Effective short-channel body factor.
- $K(W, V_{BS})$: Effective narrow-gate body factor.
- $K_1, K_3$: Body factor (first order).
- $K_2, K_4$: Body factor (second order).
- $L$: Effective channel length.
- $L_m$: Mask channel length.
- $\mu_m$: Effective channel mobility.
- $\mu_0$: Low-field mobility.
- $N_s$: Intrinsic carrier density (in atoms per cubic centimeter).
- $N_A$: Substrate doping of n-channel LDD MOSFET (in atoms per cubic centimeter).
- $\Phi_s$: Electrostatic potential at the oxide-silicon interface.
- $q$: Magnitude of electron charge (in coulombs).
- $Q_B(y)$: Bulk charge per unit area.
- $Q_C(y)$: Channel carrier charge per unit area.
- $Q_G(y)$: Gate charge per unit area.
- $R$: Half of the total drain-source resistance at $V_{DS} = 0$.
- $R_S(R_D)$: Source (drain) resistance of the n$^+$ region.
- $R_{T}(R_T)$: Source (drain) resistance of the n$^-$ region.
- $\sigma$: Drain-induced barrier lowering (DIBL) factor.
- $T$: Device temperature (in degrees Kelvin).
- $\theta$: Mobility degradation factor in the direction perpendicular to the channel current.
- $f_{ox}$: Gate oxide thickness.
- $V_{BIN}$: Effective quantity of $V_{FB} + \Phi_s$.
- $V_{BS}$: Back-gate bias (in volts).
- $V_F$: Equilibrium Fermi potential in the semiconductor bulk measured from the intrinsic Fermi potential position.
- $V_{FB}$: Flat-band voltage.
- $V_{DS}$: Internal saturation voltage.
- $V_{DSAT}$: External saturation voltage.
- $V_{GS}(V_{DS})$: Gate (drain)-to-source voltage of intrinsic MOS device.
- $V_T$: Gate (drain)-to-source voltage of intrinsic MOS device.
- $V_T$: Flat-band voltage.
- $V(y)$: Electron quasi-Fermi potential.
- $V_T$: Effective threshold voltage of MOSFET's extracted from terminal $I_D-V_{GS}$ characteristics.
- $v(y)$: Carrier drift velocity.
- $u_{max}$: Maximum carrier velocity.
- $V_s$: Saturation velocity.
- $W$: Effective channel width.
- $x$: Depth or thickness direction of the channel.
- $y$: Length direction of the channel.
I. INTRODUCTION

WITH the increasing needs in high packing density and the scaling of MOS devices towards submicrometer range, conventional MOS devices will suffer serious reliability problem due to the high field in the channel and near the drain regions. Therefore, a lightly doped drain (LDD) structure MOSFET [1], [2] has been developed for improving the device performance. It has proved to be a promising device for feature size devices in the present and future MOS-VLSI designs since the device performance has been greatly improved. This includes an increase in the breakdown voltage, better threshold-voltage characteristic, reduced hot-carrier effects, and reduced substrate and gate currents in comparison with those of conventional MOS devices. In the past, much work has focused on the study of \( I-V \) characteristics of short-channel MOSFET’s. The SPICE3 program provides four built-in MOS transistor models in which a recent one, called BSIM [3], was developed based on a semi-empirical approach and has proved to be a good one for uniformly doped short-channel devices but not for devices with implanted channel. Also, the narrow-gate (or width) effect is not included in BSIM. In contrast, studies of the \( I-V \) characteristics of LDD MOSFET’s are quite few [4]-[6]. The complete \( I-V \) characteristics of small-geometry LDD MOSFET’s considering the three-dimensional (3-D) effect, which includes both the short-channel and narrow-gate effects, have also not been reported so far. Therefore, this paper will focus on developing a new unified \( I-V \) model for short-channel and narrow-gate LDD MOSFET’s.

Several key issues for modeling the \( I-V \) characteristics of LDD MOSFET’s include the threshold voltage [6], mobility degradation, and channel length modulation effects [4], [6], and the drain–source series resistance [4], [6], [7]. It will become more difficult to obtain an analytical expression of the threshold voltage for devices with complicated device structure and process, such as a non-uniformly doped substrate, using the conventional charge sharing scheme. A simple or computational efficient threshold-voltage model for LDD MOSFET’s is not available so far. It is also well known that a channel or field implant has been used to improve the device performance for the present LDD MOSFET technology, particularly for submicrometer devices. The analytical threshold-voltage models in either existing models in SPICE3 for conventional MOSFET’s or previous models [6] for LDD MOS devices are developed based on the charge sharing scheme and can be applied to devices with either uniform substrate doping or specific doping profile only. This results in a low degree of accuracy for predicting the threshold voltage of LDD MOSFET’s with complicated device structure and implanted channel. To circumvent this problem, a simple and accurate physically based threshold-voltage model of small-geometry LDD MOSFET’s will first be developed based on a new semi-empirical approach.

The method for determining the drain–source resistance of conventional MOSFET’s was described by Suciu and Jonston [8]. However, the introduction of \( n^- \) regions in an LDD device increased the drain–source resistance, and hence, the method was inaccurate. Therefore, different approaches have been employed to determine this resistance effect [4], [7]. It will be shown in this paper that the drain–source resistance can be approximated very well by using suitably chosen boundary conditions. On developing the \( I-V \) characteristics of LDD devices, Duvvury et al. [4] were the first to develop an analytical \( I-V \) model with emphasis on the study of drain–source series resistance. Later, Lai and Sun [5] also presented an analytical \( I-V \) model, in which the drain current cannot be obtained from the terminal voltages. This prevents it from being useful as an analysis tool for circuit simulation. A recent model by Huang and Wu [6] considered the \( n^- \) region as a buried-channel MOSFET device embedded in the channel. However, the complicated expressions in the model and the associated extraction procedure made it difficult to implement in SPICE, and thus, not suitable for CAD applications. The final goal in this research is to develop a circuit simulation \( I-V \) model which is simple and easy to use for computer-aided design of integrated circuits.

In this paper, we propose a new semi-empirical model of the \( I-V \) characteristic for LDD MOSFET’s, which includes both the short-channel and narrow-gate effects. It was built upon the LEVEL3 MOS model but with several different physical parameters and extraction procedures such as the threshold voltage, body-effect coefficient, velocity saturation, channel length modulation, and drain-source series resistance effects. A consistent method for determining the device parameters is deduced from the experimentally measured \( I-V \) curves, and thus, the present model is essentially semi-empirical in nature and process-oriented. The model equations allow efficient and simple extraction of device parameters from a set of test devices. A new threshold-voltage model of small-geometry LDD MOSFET’s with implanted channel is first developed and given in Section II. Formulation of \( I-V \) equation and the associated extraction methods are developed in Section III. Continuity of the \( I-V \) characteristics from the linear to saturation regions is guaranteed by using a suitably chosen boundary conditions. Section IV presents the verification of the present model with the experimental results. A summary and conclusion are given in the last section.

II. THRESHOLD-VOLTAGE MODEL OF SMALL-GEOMETRY DEVICES

Threshold voltages is the key parameter of silicon VLSI devices. In general, two approaches can be used for analyzing the various geometry effects on the threshold-voltage variation in two dimensions or three dimensions. One is based on the charge sharing scheme by geometrical approach [9], and the other is based on the simulation of semiconductor equations [10], [11]. Numerous studies have been performed to analytically model the threshold
voltage using the charge sharing scheme. However, they have limited applications in the present CMOS technology for several reasons. One of the most important reasons existing in SPICE is that the threshold voltage of small-geometry MOSFET’s can be applied to MOS devices with uniform substrate doping only. Second, only a few studies [12], [13] have been developed to model the threshold voltage of MOSFET’s with implanted channel based on the so called box-approximation of nonuniformly doped substrate. Nevertheless, these models are device structure or process dependent. In other words, different implant conditions will have different formulations. This makes the modeling more difficult for complicated device structures or processes, particularly for LDD MOSFET’s. The above drawbacks can be overcome by using the semi-empirical approach developed in this paper in which model parameters are built upon experimentally measured data rather than from the simple charge sharing scheme. On the other hand, due to the inadequacy of the threshold-voltage model for narrow-gate MOSFET’s widely used in SPICE [14], a unified approach for achieving a simple and accurate threshold-voltage model for both short-channel, narrow-gate, and small-geometry MOSFET’s will be presented.

Short-channel and narrow-gate n-channel enhancement-mode LDD MOSFET’s with LOCOS gate structure were modeled in this paper. The experimental n-channel LDD MOS devices were fabricated using standard poly-Si gate CMOS process. One set of short-channel devices has various channel lengths from 1.5 to 12 µm with a fixed gate width of 55 µm. Another set of narrow-gate devices has channel widths from 2 to 12 µm at a fixed channel length of 15 µm. Several small-geometry devices with different aspect ratios (W/L) are also provided. The silicon wafers used were (100) orientation and the resistivity ranged from 15 to 25 Ω·cm. The shallow and deep implants were carried out using energies of 25 and 150 keV and doses of 7.5 × 10^15/cm^2 and 4 × 10^15/cm^2, respectively. The n⁺ source and drain junctions were formed by using As⁺ implant through a thin oxide (250 Å) with an energy of 60 keV and a dose of 6 × 10^15/cm^2. The n⁻ LDD structures were formed by implanting As⁺ ions with an energy of 30 keV and a dose of 3 × 10^15/cm^2. Gate oxide was measured to be 280 Å. The field oxide thickness was 4900 Å. N⁺ source and drain junction depths are 0.31 µm and those of n⁻ regions are 0.2 µm. The spacer width is 0.2 µm. A GPIB-based IBM PC and a HP 4145B picoampere meter were used for I-V measurements.

A. Short-Channel Effect

From the charge sharing method, the threshold voltage \( V_T \) of a short-channel n-MOSFET with uniform substrate doping can be expressed by

\[
V_T = V_{FB} + \Phi_S + \kappa F \sqrt{\Phi_S - \Phi_{BS}} - \sigma V_{DS}
\]  

(1a)

where

\[
\kappa = \sqrt{2q\epsilon_s N_A/C_{ox}}.
\]  

(1b)

is the body factor; \( F \) is the charge sharing factor which approaches value of one for a long-channel device; \( \sigma \) accounts for the drain-induced barrier lowering (DIBL) effect; \( V_{FB} \) is the flat-band voltage; \( \Phi_S \) is the surface potential; \( \epsilon_s \) is the permittivity of the silicon; \( N_A \) is the substrate doping; and \( C_{ox} \) is the gate oxide per unit area. Fig. 1 is the measured \( V_T \) versus \( \Phi_S - \Phi_{BS} \) results for a set of short-channel devices (lower three curves) and a set of narrow gate devices (upper three curves). The threshold voltage of short-channel device decreases with reducing channel length. Note that \( V_T \) is proportional to the first order of \( (\Phi_S - \Phi_{BS})^{1/2} \) for devices with uniform substrate doping. However, from measured results (lower three curves), their threshold voltages are proportional to the second order of \( (\Phi_S - \Phi_{BS})^{1/2} \) for devices with implanted channel. Therefore, for long-channel and short-channel devices with implanted channel, we may define their threshold voltage as the following:

\[
V_T = V_{BIN} + K_1 \sqrt{\Phi_S - \Phi_{BS}} - K_2 (\Phi_S - \Phi_{BS}) - \sigma V_{DS}
\]  

(2)

or

\[
V_T = V_{BIN} + K_1 (L, V_{BS}) \sqrt{\Phi_S - \Phi_{BS}} - \sigma V_{DS}
\]  

(3a)

where

\[
K_1 (L, V_{BS}) = K_1 - K_2 \sqrt{\Phi_S - \Phi_{BS}}.
\]  

(3b)

Here, \( V_{BIN} = V_{FB} + \Phi_S \) using the notation as given in SPICE2. \( K_1 \) and \( K_2 \) terms are two body factors, in which \( K_2 \) exists due to the channel implants. \( K_1 (L, V_{BS}) \) is defined as the effective short-channel body factor which accounts for the short-channel and channel implantation effect. These four parameters, \( V_{BIN}, K_1, K_2, \) and \( \sigma \), can be determined experimentally by fitting the threshold voltages of MOSFET’s on a set of test samples having various channel lengths. Note that the above threshold voltage expression, (2) or (3a), is valid for both LDD and conventional MOSFET’s.

![Fig. 1. Measured threshold voltages for LDD MOSFET’s with various channel widths and lengths at V_{DS} = 0.1 V. (□)—narrow-gate devices, (+)—short-channel devices.](image-url)
B. Narrow-Gate Effect

As the device channel width becomes narrower, the threshold voltage will increase with reducing gate width. For the same reasoning as in [14], the threshold voltage of a narrow gate but long channel device is given by

\[ V_T = V_{T(longL)} + \Delta V_T \]  (4a)

where

\[ V_{T(longL)} = V_{BS1} + K_3(L = \infty, V_{BS})\sqrt{\Phi_S - V_{BS}} \]  (4b)

and

\[ \Delta V_T = K_W(W, V_{BS})\sqrt{\Phi_S - V_{BS}}. \]  (4c)

Here, \( K_W(W, V_{BS}) = K_3 + K_4\sqrt{\Phi_S - V_{BS}} \) is called the effective narrow-gate body factor for narrow-gate MOS devices. \( K_3 \) and \( K_4 \) are the first- and second-order body factors due to the narrow-gate effect which can be determined experimentally. \( K_W \) accounts for the width effect and the doping encroachment caused by the field implants.

C. Small-Geometry Effect

Our new threshold-voltage expression for a small-geometry MOSFET can be obtained by superposing both short-channel and narrow-gate effects, which is obtained by incorporating (3a) and (4a)-(4c), and gives

\[ V_T = V_{BS1} + K_3(L, V_{BS})\sqrt{\Phi_S - V_{BS}} + K_W(W, V_{BS})\sqrt{\Phi_S - V_{BS}} - aV_{DS}. \]  (5)

Here, we developed the short-channel effect and narrow-gate effect independently and their combined effect gives the above formulation. But as will be shown later, (5) is valid for small-geometry devices down to the submicrometer range.

D. Extraction of Model Parameters

The threshold voltages are obtained from the measured device terminal characteristics as illustrated in Fig. 2. At low drain voltages (e.g., \( V_{DS} = 0.1 \) V), the threshold voltage is defined by finding the maximum slope of the \( I_D-V_{GS} \) curve extrapolated to zero current, intersecting the \( V_{GS} \) axis at \( V_T \) where \( V_T \) is determined. Note that the maximum tangent is taken because, at that point, the mobility degradation effect is minimum and can be neglected. For high drain voltages, \( V_T \) is defined as the intercept of the maximum extrapolated tangent of the \( \sqrt{I_D} - V_{GS} \) curve with the \( V_{GS} \) axis. Determination of the threshold-voltage parameters will be described as follows.

1) \( \Delta L, \Delta W \): In the characterization of \( V_T \) versus channel length characteristics, effective channel length \( L \) has to be known first, where \( L = L_m - \Delta L \). \( L_m \) is the mask channel length and \( \Delta L \) is the channel length reduction. Fig. 2 also shows the variation of transconductance versus gate voltage \( V_{GS} \) which is defined by \( G_m = (\partial I_D/\partial V_{GS}) \) at small \( V_{DS} \). From the \( I_D-V_{GS} \) characteristics of short-channel MOSFET’s, the maximum value of transconductance \( G_{m(max)} \) is related to the mask channel length by

\[ G_{m(max)}^{-1} = (L_m - \Delta L)/[\mu_0 C_{OS}(W_m - \Delta W)V_{DS}]. \]  (6)

In practice, \( G_{m(max)} \) is determined as the maximum slope of the \( I_D-V_{GS} \) curve at small \( V_{DS} \). Measurement of the \( I_D-V_{GS} \) curves for various channel length \( (L_m) \) devices gives the plot of \( G_{m(max)} \) versus \( L_m \) as shown in Fig. 2, in which the intercept of the curve with the \( L_m \) axis gives \( \Delta L = 1 \) \( \mu m \). Channel width reduction \( \Delta W \), due to the bird’s beak and field implant encroachment, can be extracted in a similar manner by plotting \( G_{m(max)} \) versus \( W_m \) for a set of narrow gate devices, which then gives the intercept of the curve with the \( W_m, \Delta W = 1.3 \) \( \mu m \).

2) \( a \): In determining the DIBL factor \( a \), variations of \( V_T \) with \( V_{DS} \) can be obtained from the family of curves \( I_D-V_{GS} \) at different \( V_{DS} \). A typical result is shown in Fig. 3, in which \( V_T \) is plotted against \( V_{DS} \) and the slopes give the values of \( a \). Variation of \( a \) with effective channel length can be obtained by an exponential fitting, as given in Fig. 4. This shows an increase of \( a \) with reducing channel.
length, which is consistent with the fact that short-channel device has larger DIBL.

3) $V_{BIN}$, $K_1$, and $K_2$: For the sake of simplicity and the same reasons as given in [15], $\Phi_2 = 2V_F$ (where $V_F$ is the quasi-Fermi potential) is used and $V_F = (kT/q) \ln \left( \frac{N_D}{N} \right)$. Instead of using a direct second-order fitting of (2) to find $K_1$ and $K_2$ as in BSIM [3], we propose a new approach by first finding $V_{BIN}$ from curve 4 in Fig. 1 and then calculating values of $K_L$ from (2a), i.e.,

$$K_L(L, V_{BS}) = \left( V_T - V_{BIN} + \sigma V_{DS} \right) / \sqrt{\Phi_2 - V_{BS}} = K_1 - K_2 \sqrt{\Phi_2 - V_{BS}}$$

(7)

where $V_{BIN}$ is assumed to be constant for each device. Plotting of $K_L(L, V_{BS})$ versus $\sqrt{\Phi_2 - V_{BS}}$ gives a family of straight lines as shown in Fig. 5, from which $K_1$ and $K_2$ for various channel lengths can be determined. $K_2$ is the slope of the curve which shows the channel implantation effect. It is noted that the nonzero slopes of these curves show the effect of channel implants since $K_2 = 0$ for devices with uniform substrate doping. Fig. 5 also reveals that values of $K_L(L, V_{BS})$ decrease with decreasing channel length at a fixed $V_{BS}$. This factor takes into account the short-channel effect and the channel implantation effect which is consistent with the results from the simple charge sharing concept. In other words, in the charge sharing scheme, $F$ decreases with reducing channel length as does for $K_L(L, V_{BS})$. Finally, variations of $K_1$ and $K_2$ with effective channel length are shown in Fig. 6, in which an excellent match can be obtained by matching the computed data with an exponential fit.

4) $K_3$, $K_4$: $K_3$ and $K_4$ can be determined from the upper family of curves in Fig. 1 for narrow-gate devices. Using the bottom curve (curve 3, $W_m = 12 \mu m$) as the reference and taking the difference of the values between this and any of the other curves, the threshold-voltage shifts ($\Delta V_T$) for different gate width devices as function of back-gate biases are thus computed. Again, based on (4a), $K_w$ can be determined and its plot against $\sqrt{\Phi_2 - V_{BS}}$ gives Fig. 7 with gate width as a varying parameter. Finally, variations of $K_3$ and $K_4$ as functions of channel width can be plotted and fitted as shown in Fig. 8. The increase of $K_3$ and $K_4$ with reducing channel width is consistent with the fact that narrow-gate MOS device has higher threshold voltage. Note that $K_w$ approaches zero for large $W$ which means that there is zero threshold voltage shift, (4a), for a wide gate (very large $W$) device.
The present I-V model is built upon LEVEL3 MOS model with many modifications such as the saturation voltage, velocity saturation, channel length modulation, and drain–source series resistance effects. An LDD MOS device can be considered to be an intrinsic MOSFET in series with two explicit resistors as shown in Fig. 9.

A. The Linear Region

In LEVEL3, the drain current of a MOSFET in the linear region is given by the equation

$$I_D = \beta \left[ (V_{GS} - V_T) - 0.5aV_{DS} \right]V_{DS} \quad (8a)$$

where

$$\beta = \beta_0/(1 + \theta(V_{GS} - V_T))(1 + \eta V_{DS}) \quad (8b)$$
$$\beta_0 = \mu_0 C_{ox}(W/L) \quad (8c)$$
$$a = 1 + \frac{0.5g(K_1 + K_3)}{\sqrt{\Phi_S - V_{BS}}} - (K_2 - K_4) \quad (8d)$$
$$g = 1 - \frac{1}{1.744 + 0.836(\Phi_S - V_{BS})} \quad (8e)$$

Here, $a$ is the body-effect charge sharing factor. It is worth noting that the expression has an additional term, $K_2-K_4$, which is different from that in BSIM. This is caused by the introduction of a second-order body-effect term in (3b). A detailed derivation of $a$ is given in the Appendix. $\theta$ is the vertical-field mobility degradation factor. $\eta$ is another degradation factor caused by the velocity saturation effect. $\mu_0$ is the low-field mobility.

For LDD MOSFET’s, the above expression is not valid due to the significant contribution of the drain–source series resistance in the n− region to the device I-V characteristic. This series resistance will cause mobility degradation and induce lower drain current in the linear region, and thereby gives less current driving capability. Consequently, this resistance effect cannot be modeled simply by the mobility degradation factor $\theta$ alone, such as the method in [8] for conventional MOSFET’s.

Duvvury et al. [4] suggest one way of including the series resistance in the current expression by an empirical form for this resistance from linear to saturation operating regions. A similar scheme with modified boundary conditions but a more accurate approach will be used here and described as follows.

For the intrinsic MOSFET, its drain current is given by

$$I_D = \beta_0(V_{GS} - V_T - 0.5aV_{DS})V_{DS}/\left[ (1 + \theta(V_{GS} - V_T))(1 + \eta V_{DS}) \right]. \quad (9)$$

Therefore, we have the expression

$$R_T = 2R + r'_{ch} \quad (10)$$

for the total measured resistance between drain $D$ and source $S$, where $r'_{ch} = V_{DS}/I_D$ and can be obtained from (9); $R_T = V_{DS}/I_D$; $R = R_s + r_s$ (or $R_D + r_d$); $R_s (R_D)$ is the resistance of the n+ source (drain) region; and $r_s (r_d)$ is the resistance of the n− source (drain) region. Also, we have the terminal relations

$$V'_{GS} = V_{GS} - RI_D \quad (11a)$$
$$V'_{DS} = V_{DS} - 2RI_D. \quad (11b)$$

Combining (9)–(11) gives an implicit expression of $I_D$ which can be solved by using iterations. In order to save computation time and express $I_D$ analytically in terms of terminals for simulation application, the drain current expression is approximated as follows.

The total resistance between the drain and source terminals, (10), can be rewritten as

$$R_T = 2R + r'_{ch} + \Delta r \quad (12)$$

where

$$r'_{ch} = 1/\beta(V_{GS} - V_T - 0.5aV_{DS}) \quad \text{and} \quad \Delta r = r_{ch} - r'_{ch}.$$
channel resistance difference \( \Delta r \) is known. \( \Delta r \) can be obtained by the two boundary conditions at \( V_{DS} = 0 \) and \( V_{DSAT} \) as follows. At very low drain voltage, as \( V_{DS} \to 0 \), \( r'_{th} \ll 2R \), and \( r_{ch} \ll 2R \), so \( \Delta r = 2R \). At the saturation point when \( V_{DS} = V_{DSAT} \), \( \Delta r \) can be obtained by setting (12) equals to (16) (shown later) to retain continuity of the current at the saturation point, which gives

\[
\Delta r = RV_{dsat}/(V_{GS} - V_T - 0.5aV_{DSAT}),
\]

at \( V_{DS} = V_{DSAT} \).

Then, the expression of \( \Delta r \) as a function of drain voltage in the linear region can be approximated by an empirical form as

\[
\Delta r = 2R - R_c(V_{DS}/V_{DSAT}).
\]

where

\[
R_c = RV_{dsat}/(V_{GS} - V_T - 0.5aV_{DSAT}).
\]

Combining (9), (12), and (14), we have

\[
I_D = \beta_0(V_{GS} - V_T - 0.5aV_{DS})V_{DS}/
\]

\[
[(1 + \theta(V_{GS} - V_T))(1 + \eta V_{DS})
\]

\[
+ R_c(V_{DS}/V_{DSAT})\beta_0(V_{GS} - V_T - 0.5aV_{DS})].
\]

(15)

Therefore, \( I_D \) can be computed directly from the device terminal voltages.

**B. The Saturation Region**

For short-channel LDD devices, the drain voltage corresponding to the onset of saturation is determined by the requirement that the lateral electric field is at its critical value, \( E_C \), at the pinchoff point, where electrons will attain their limit velocity. To find an expression for the saturation voltage \( V_{dsat} \), we equate the current calculated from the linear portion of the channel with the current at the pinchoff point. The saturation current at the pinchoff point is given, from (9), by

\[
I_{dsat} = \beta(V_{GS} - V_T - 0.5aV_{dsat})V_{dsat}
\]

or

\[
I_{dsat} = \beta(V_{GS} - V_T - 0.5aV_{dsat})V_{dsat}/(1 + \beta RV_{dsat}).
\]

(16)

The saturation current at pinchoff point can also be expressed by

\[
I_{dsat} = \mu_n WC_{ox} [V_{GS} - V_T - 0.5aV_{dsat}]E_C
\]

which is again expressed in terms of terminal voltages by

\[
I_{dsat} = \mu_n WC_{ox} [V_{GS} - V_T - 0.5aV_{dsat}]E_C
\]

\[
= \mu_n WC_{ox} [V_{GS} - V_T - 0.5aV_{dsat}](1 + \eta V_{DS}).
\]

(17a)

where \( \mu_n = \mu_0/(1 + \theta(V_{GS} - V_T))(1 + \eta V_{DS}) \).

(17b)

Equating (16) and (17a) gives

\[
I_{dsat} = I_D \cdot (1 - \delta L/L).
\]

(18)

where \( \delta L \) is the channel length reduction due to channel length modulation effect. However, with the addition of \( n^- \) regions between \( n^+ \) regions, \( \delta L \) has a somewhat different form from that of LEVEL3. Here, the expression of \( \delta L \) in [4, eq. (C13)] is used in this paper.

**C. Extraction of Model Parameters**

1) Determination of \( \mu_0, \theta, \text{and } R \): For small value of \( V_{DS} \) and high value of gate voltages \( V_{GS} \gg I_D R \), the voltage across the \( n^- \) regions can be neglected so that \( V_{GS} \equiv V_{DS} \) and \( V_{DS} \equiv V_{DS} \). \( \mu_0 \) and \( \theta \) can be determined from the linear region \( I_D-V_{GS} \) characteristics. In such a case, combining (7) and (8) gives

\[
R_T = V_{DS}/I_D = 2R + [1/\beta_0][(V_{GS} - V_T)^{-1} + \theta].
\]

(19)

Plotting of \( R_T \) versus \( (V_{GS} - V_T)^{-1} \) for a set of transistors with different channel lengths, a family of curves is obtained as shown in Fig. 10. Using least square fit, the slope of these curves is \( 1/\beta_0 \) and the intercept with the vertical coordinate is \( R_0 \), where \( R_0 = 2R + \theta/\beta_0 \). From the top curve for a long channel device, \( L_m = 12 \mu m \), its slope gives \( \mu_0 = 512.7 \text{ cm}^2/\text{V} \cdot \text{s} \). If we again plot \( R_0 \) versus \( 1/\beta_0 \), least square fit gives the slope \( \theta \) and the intercept \( R \) as shown in Fig. 11.

2) Determination of \( \eta \): To obtain horizontal field degradation factor \( \eta \), the \( I_D-V_{GS} \) data for different drain voltages are used. Rearranging (18) gives

\[
H = I_D [1 + \theta V_{DS}]/V_{GS}
\]

\[
= \beta_0 (V_{GS} - V_T - 0.5aV_{DS})/(1 + \eta V_{DS}).
\]

(20)

Fig. 12 shows the family of curves of \( H - V_{GS} \) for a device with \( L_m = 3 \mu m \). In the high gate voltage region, the
IV. COMPARISONS BETWEEN EXPERIMENTAL AND MODELED RESULTS

Based on the proposed model equations, parameter extraction, and a number of device characteristics obtained above, this section will be devoted to comparisons of the experimental results and modeled results as well as a discussion of the comparisons with reported models.

Fig. 15(a) and (b) shows the comparison between the measured and modeled threshold voltages for short-channel and narrow-gate devices at various bias conditions. Excellent agreements are achieved. The threshold-voltage model for small-geometry devices is developed independently and then combined together. The modeled values of the threshold voltages from this model are also in good agreement for transistors with various aspect ratios as shown in Fig. 16. Note that, without resorting to complicated formulations as shown in [13] and [14], we are able to use the simple formulas (3), (4) and (5) to predict the threshold voltages of short-channel, narrow-gate, and small-geometry LDD MOSFET's with implanted channel, respectively. Also, the simple formulation of the threshold-voltage model is especially suitable for CAD applications.
The dc $I_D-V_{GS}$ characteristics for different channel length, width, and small-geometry LDD devices are shown in Fig. 17(a)-(d), in which comparisons have also been made for the measured (solid lines) and modeled (dotted circles) results with effective channel length (width) down to the submicrometer range. It was shown that reasonable agreement has been achieved, which strongly supports the validity of the model equations. Several improvements in this work will be described and compared with reported models as follows.

1) The simplified expression of the threshold voltage and the associated $I-V$ model are greatly enhanced for CAD applications. Particularly, the threshold-voltage model of small-geometry LDD MOSFET's, which was previously unavailable in SPICE2, has been successfully implemented for the first time. It has also been tested that the proposed threshold voltage expressions are valid for conventional MOSFET's as shown elsewhere [16].

2) In deriving the $I-V$ equation, we put the factors $K_2$, $K_3$, and $K_4$ into the expressions of $"a","$ which was neglected in BSIM. By doing so, the influences of back-gate bias effect on the $I-V$ characteristics due to the channel implantation effect and small-geometry effect can be clearly demonstrated.

3) Concerning the velocity saturation effect, the SPICE LEVEL3 model uses the parameter $\eta$ to account for it, while Wong and Salama [17] added another empirical parameter, DEL, to improve the accuracy. However, the value of $\eta_{max}$ is not directly extracted from the devices under investigation, which violates the consistency of the proposed model. To rule out this drawback, the parameter $\eta$ is better employed by an empirical form as shown in Fig. 13 in the present model to deal with this effect so that accuracy can be improved.

4) In BSIM [3] or most of the reported method [6], [8], the drain-source resistance is lumped into the mobility degradation factor $\theta$. Unfortunately, this will approximate the $I-V$ characteristics very well at the small $V_{DS}$ only. In this paper, the drain-source series resistance expression is assumed to be constant at small drain voltage and is approximated by a function of $V_{DS}$ in the device linear operating region. Although accuracy can be improved by considering the gate voltage dependence of the drain-source series resistance [7], this will increase CPU time for circuit simulation application. To make a trade-off between CPU time and accuracy, constant drain-source series resistance is used. Also, the continuity of the output conductance at the saturation point is ensured by a suitably chosen boundary condition. However, in reported results by Huang and Wu [6], overestimation of the drain current at the saturation point will give rise to the discontinuity of output conductance at the saturation point. This discontinuity will cause convergence problem when doing circuit simulation.

One important implication from the present model is that the derivations of model equations and the extraction methods are not restricted to one specific set of test samples. In other words, although the proposed threshold-
voltage and $I-V$ models in the present paper are developed from n-channel enhancement model devices, they are expected to be applicable to n-channel depletion-mode or p-channel LDD MOSFET's. Since the values of empirical parameters in the above model equations may be different for a different structure or process, the extraction of these parameters will be the same. Particularly, the proposed threshold-voltage formulation is independent of these devices since the semi-empirical model is based on experimental data and the accuracy can be assured. However, as is well known, those models for depletion devices based on the physical derivation will encounter difficulties for geometry and implantation effects. Furthermore, recent advances in the process technology have made deep-submicrometer MOSFET's mature for next-generation ULSI circuits. These devices show device characteristics similar to near-micrometer devices but with significant second-order effects [18]. Since the present model is semi-empirical, it is also expected that the submicrometer model in this paper can be extended to deep-submicrometer devices. For example, empirical parameters such as $K's$, $\theta$, $\gamma$, etc. need to be characterized for device effective channel length (width) in the deep-submicrometer range with only minor modifications in the extracted values and empirical forms.

V. Summary and Conclusion

In this paper, an accurate and computationally efficient semi-empirical $I-V$ model of a small-geometry LDD MOSFET, which has been built in a SPICE program, was proposed. The present $I-V$ model was built upon a SPICE LEVEL3 MOSFET model with many modifications. Device characteristics such as the threshold voltage and linear and saturation region currents are derived experimentally from measured device terminal characteristics and new parameter extraction procedures. The present $I-V$
model is well-suited for simulating VLSI circuits which consist of both short-channel and narrow-gate LDD MOSFET’s.

A simple and accurate semi-empirical threshold-voltage formula is first obtained which considers both the short-channel, narrow-gate, small-gate, and channel/field implantation effects. Six parameters are employed in the above model. The developed drain current can be computed directly from the device external voltages. Only 11 model parameters are used to fully adapt the small-gate I-V relation. The developed drain current for MOS devices operating in the strong inversion region can be expressed by

\[ I_D = \mu_n C_{ox}(W/L) \int_{0}^{\varphi_{FS}} \bigg [ V_{GS} - V_{FB} - \Phi_S - V_N - (K_1 + K_3) \sqrt{\Phi_S - V_{BS} + V_N} 
+ (K_2 - K_4)(\Phi_S - V_{BS} + V_N) \bigg ] dV_N \]

where

\[ F(V_{DS}, \Phi_S - V_{BS}) = \frac{(2/3) \bigg [(V_{DS} + \Phi_S - V_{BS})^{3/2} - (\Phi_S - V_{BS})^{3/2} \bigg ]}{1 - \frac{1}{1.744 + 0.836(\Phi_S - V_{BS})}} \]  

Using the above approximation, (A5a) can be reduced to (8a), and the body-effect charge sharing factor \( a \) is given in (8b).

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**APPENDIX**

The drain current of a narrow-gate MOSFET, which is similar to BSIM but in a somewhat different form, will be derived here. The drain current for MOS devices operating in the strong inversion region can be expressed by

\[ I_D = \int_0^W Q_c(y) v(y) dy \]  

where \( v(y) \) is the carrier drift velocity given by

\[ v(y) = \mu_n dV_N/dy \]  

and \( Q_c(y) \) is the carrier charge per unit area at any point in the channel.

Gate charge is given by

\[ Q_{G}(y) = C_{ox}(V_{GS} - V_{FB} - \Phi_S - V_N) \]  

and the bulk charge is given effectively by

\[ Q_{B}(y) = C_{ox}K\sqrt{\Phi_S - V_{BS} + V_N} \]  

in which the effective body factor, \( K = (K_1 + K_2) - (K_2 - K_1) \sqrt{\Phi_S - V_{BS} + V_N} \) (by comparing with (5)), is used due to the contribution of the body effect caused by the channel implant and narrow-gate effect. \( Q_{G}(y) \) is then given by

\[ Q_{G}(y) = Q_{o}(y) - Q_{b}(y) = C_{ox}[V_{GS} - V_{FB} - \Phi_S - V_N - (K_1 + K_3) \sqrt{\Phi_S - V_{BS} + V_N} + (K_2 - K_4)(\Phi_S - V_{BS} + V_N)] \]  

Combining (A1a), (A1b), and (A4) and integrating (A1a) along the channel gives

\[ I_D = \mu_n C_{ox}(W/L) \int_0^{\varphi_{DS}} \bigg [ V_{GS} - V_{FB} - \Phi_S - V_N - (K_1 + K_3) \sqrt{\Phi_S - V_{BS} + V_N} + (K_2 - K_4)(\Phi_S - V_{BS} + V_N) \bigg ] dV_N \]

\[ = \mu_n C_{ox}(W/L) \{ (V_{GS} - V_{BN} + (K_2 - K_4) \sqrt{\Phi_S - V_{BS})} - 1/2 - (K_2 - K_4) \} V_{DS}^2 \]

\[ - (K_1 + K_3) F(V_{DS}, \Phi_S - V_{BS}) \} \]  

\[ F(V_{DS}, \Phi_S - V_{BS}) = (2/3) \bigg [(V_{DS} + \Phi_S - V_{BS})^{3/2} - (\Phi_S - V_{BS})^{3/2} \bigg ] \]  

\[ = \sqrt{\Phi_S - V_{BS}} + (0.25gV_{DS}^2/\sqrt{\Phi_S - V_{BS}}) \]  

where

\[ g = 1 - \frac{1}{1.744 + 0.836(\Phi_S - V_{BS})} \]

Steve Shao-Shiun Chung (S’83– M’85) received the B.S. degree from the National Cheng-Kung University, Taiwan, Republic of China, in 1973, the M.Sc. degree from the National Taiwan University, Taiwan, in 1975 and the Ph.D. degree from the University of Illinois at Urbana-Champaign in 1985, all in electrical engineering. From 1976 to 1978 he worked for an electronic instrument company as Chief of the R&D Division and subsequently as Manager of the Engineering Division. From 1978 to 1983 he was with the Department of Electronic Engineering and Technology at the National Taiwan Institute of Technology (NTIT) as a Lecturer. He was also in charge of an Instrument Calibration Center at NTIT. From 1983 to 1985 he held a research assistantship in the Solid State Electronics Laboratory and the Department of Electrical and Computer Engineering at the University of Illinois. In September 1985 he served at NTIT again as an Associate Professor in the Department of Electronic Engineering. Since August 1987 he has been with the Department of Electronic Engineering and Institute of Electronics, National Chiao Tung University, Taiwan, as an Associate Professor. His current teaching and research interests are in the areas of solid-state device physics and technology; semiconductor device and circuit modeling; process, device, and circuit simulation; characterization and reliability study of novel miniaturized MOS devices; and CAD of VLSI.

Tzang-Si Lin was born in Chiayi, Taiwan, Republic of China, on April 24, 1964. He received the B.S. and M.Sc. degrees from the Department of Electronic Engineering and Institute of Electronics at National Chiao Tung University, Taiwan, in 1986 and 1988, respectively. His master's thesis was on developing a SPICE model for short-channel MOS devices with implanted channel. His current research interests are in the area of semiconductor device physics and technology, simulation, modeling, and hot-carrier study of miniaturized MOS devices.

Yuh-Gong Chen was born in Hualien, Taiwan, Republic of China, on August 17, 1956. He received the B.S. degree from the Department of Electrical Engineering, Feng-Chia University, in 1980 and the M.Sc. degree from the National Taiwan Institute of Technology in 1988. He was an Assistant Engineer in the Chung-Shan Institute of Technology during 1980–1982. He joined Winbond Electronic Corporation at the Hsinchu Industrial Park, Taiwan, as an Assistant Engineer, in August 1988. Since March 1989 he has been with Silicon Integrated Systems Corporation at the Hsinchu Industrial Park, Taiwan, working on MOS/VLSI device and technology development.