



The Strong Degradation of 30 Å Gate Oxide Integrity Contaminated by Copper

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A much higher leakage current, a lower breakdown effective field, a poorer charge-to-breakdown, and worse stress-induced leakage current are observed in ultrathin 30 Å oxides even at a low Cu contamination of 10 ppb. The strong degradation of the ultrathin gate oxide integrity can be explained by the tunneling barrier lowering and the increased interface trap tunneling due to the presence of Cu in the oxide and at the oxide-Si interface.

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Cu contamination¹⁻⁷ has attracted much attention in advanced high-speed complementary metal oxide semiconductors (CMOS) circuits using Cu metallization. The Cu contamination, which may come from either the front surface Cu interconnects or the back-side surface contaminated by the Cu process, may precipitate at the Si/SiO₂ interface^{5,7,8} or form a silicide by a reaction with Si. The Cu contamination can degrade metal oxide field effect transistor's (MOSFETs) performance by increasing the leakage current at the source-drain junction, shifting the threshold voltage, and increasing the subthreshold swing.^{8,9} The Cu contamination may also degrade the gate oxide integrity by reducing the breakdown electric field at high contamination levels,² but has little effect on the gate area oxide breakdown at low contamination levels.¹ However, most of the reported Cu contamination studies are focused on relatively thick oxides. In this paper, we have examined the gate oxide integrity¹⁰⁻¹² of Cu-contaminated ultrathin ~30 Å oxides used for an 0.18 μm generation. In contrast to previous reports on thick oxides, we have found severe degradation of the gate oxide integrity for these ultrathin ~30 Å oxides. Compared with the control sample, the contaminated oxides show higher direct and Fowler-Nordheim (F-N) tunneling currents, lower breakdown electric field, poorer charge-to-breakdown distribution (Q_{BD}), and worse stress-induced leakage current (SILC), even at a low Cu contamination level of 10 ppb. This is probably due to the presence of Cu within both the oxide and the Si-oxide interface, which effectively lowers the tunneling barrier and increases the SILC.

Experimental

Standard 4 in. p-type Si (100) wafers with a typical resistivity of ~10 Ω cm were used in this study. The preoxidation cleaning of the wafers was performed by a modified RCA clean, followed by HF dipping, and spin drying. Device isolation was formed by growing and patterning the 3000 Å thick field oxide. Then the ~30 Å gate oxide was grown at 900°C in dry oxygen diluted with nitrogen. The oxide thickness was measured by ellipsometry and high frequency C-V measurements under accumulation. The gate electrode was formed by depositing a 3000 Å poly-Si with subsequent phosphorus doping by POCl₃. The standard aluminum contact was formed by thermal evaporation, and MOS capacitors of 100 × 100 μm were fabricated. The Cu contamination was introduced by dipping the devices for 1 min into a CuSO₄ solution with a concentration of 10 ppb or 10 ppm, and the contaminated wafer was then annealed at 400°C in a nitrogen gas ambient.

Results and Discussion

Figure 1a and b show the current density-voltage (J-V) characteristics of MOS capacitors with 30 and 50 Å oxides, respectively.

For the thick 50 Å oxide, the Cu contamination slightly increases the gate oxide leakage current in the pretunneling region, which may be attributed to the trap-assisted tunneling. The reason why the Cu contamination has little effect on the F-N tunneling may be due to a much larger current conduction than the trap-assisted tunneling at large bias. In contrast, a large leakage current is also observed in the direct tunneling region in addition to the increased pretunneling current. The two orders of magnitude larger leakage current at direct tunneling regime is unacceptable for low power circuit application. If a thinner oxide has a similar increasing trend for the leakage

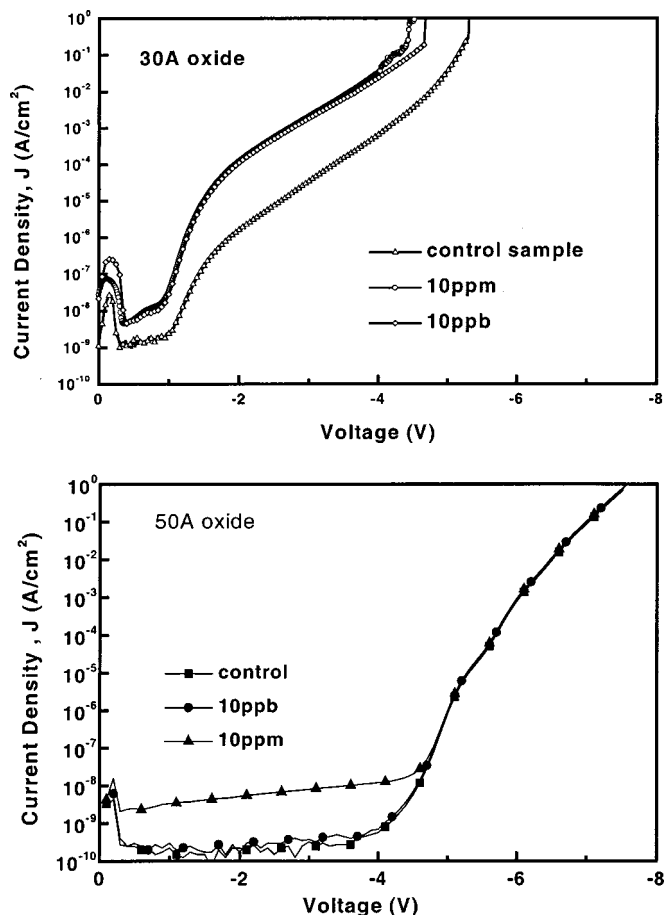


Figure 1. J-V characteristics of MOS capacitors with (a, top) 30 Å and (b, bottom) 50 Å oxides. The devices were contaminated by 10 ppb or 10 ppm Cu. A control sample without Cu contamination is also shown for comparison.

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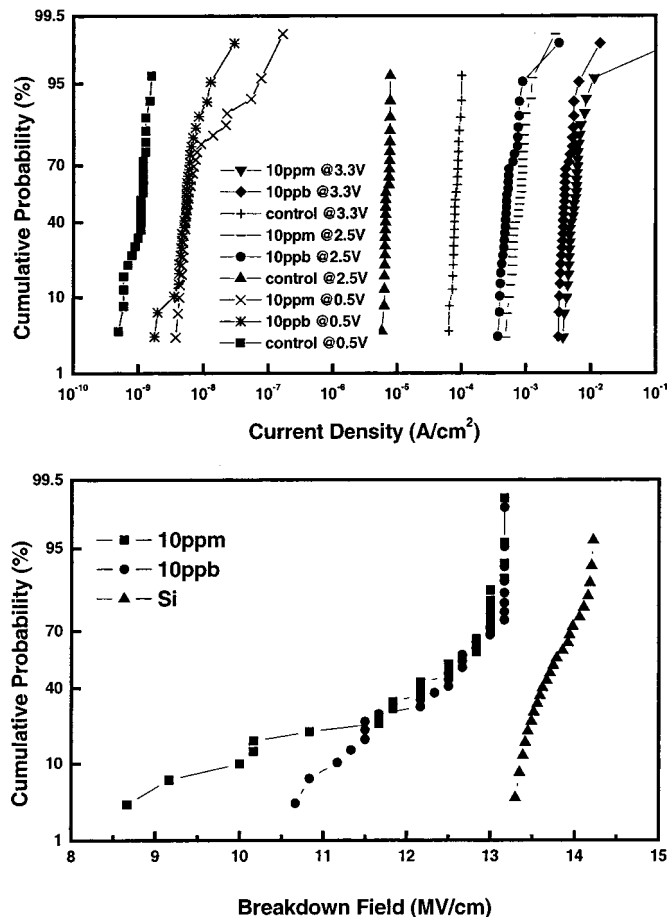


Figure 2. (a, top) The leakage current density and (b, bottom) the breakdown electric field of 30 Å oxides with different Cu contamination levels. The breakdown is defined at a current density of 10⁵ A/cm² (0.1 A through a 100 × 100 μm area).

current, then it will ultimately limit the gate oxide scaling because the allowed maximum leakage current is at 1 A/cm².¹²

To further analyze the J-V characteristics, we have plotted the leakage current and breakdown electric field in Fig. 2a and b, respectively. As shown in Fig. 2a, the leakage current is one to two orders higher in the Cu-contaminated sample than in the control sample, and the leakage current generally increases with the Cu-contamination level. The higher leakage current of Cu-contaminated MOS devices than control samples suggests a higher defect density inside the oxide. According to the lattice-damage model, defects with a higher density in the oxide will grow faster and finally generate a current conduction path that will have a very high energy density and cause oxide breakdown.¹³ Therefore, the higher leakage current in Cu-contaminated samples is expected to be correlated with a lower breakdown electric field. This is further evidenced from the lower cumulative breakdown field of Cu-contaminated samples shown in Fig. 2b, where the breakdown is defined at a current density of 10³ A/cm². It is important to notice that no such effect of lowering the breakdown field was found in the thick 50 Å oxide as shown in Fig. 1b and in agreement with the literature regarding low Cu contamination.¹

Figure 3 shows the Q_{BD} distribution of ultrathin ~30 Å oxides. The standard oxide without contamination has a mean Q_{BD} of ~0.13 C/cm² at a constant voltage stress of -4.3 V, which is close to the data published in the literature.¹⁴ The Cu-contaminated MOS capacitor has a larger Q_{BD} distribution than the control device, and this is consistent with the larger distribution of leakage current and

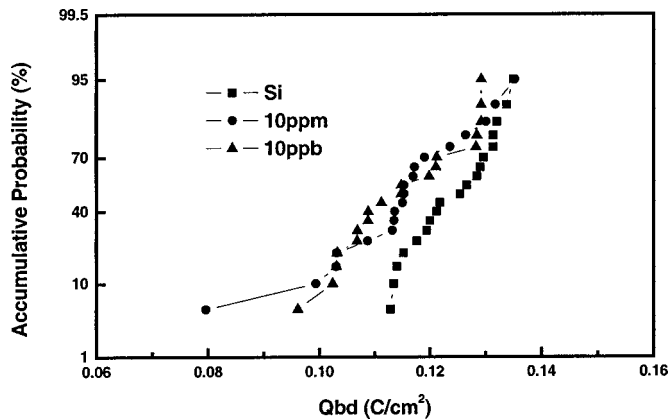


Figure 3. The Q_{BD} distribution at -4.3 V constant voltage stress of ultrathin 30 Å oxides with different Cu contamination level.

the breakdown electric field shown in Fig. 2a and b. The larger Q_{BD} distribution might be due to a wide variation of the Cu concentration inside the oxide. In addition to the larger distribution, the Cu-contaminated MOS capacitor has a lower Q_{BD} value than the control device. The larger Q_{BD} distribution in combination with a lower Q_{BD} for the capacitor contaminated with 10 ppm Cu than the one contaminated with 10 ppb Cu may be due to the higher Cu concentration inside the oxides.

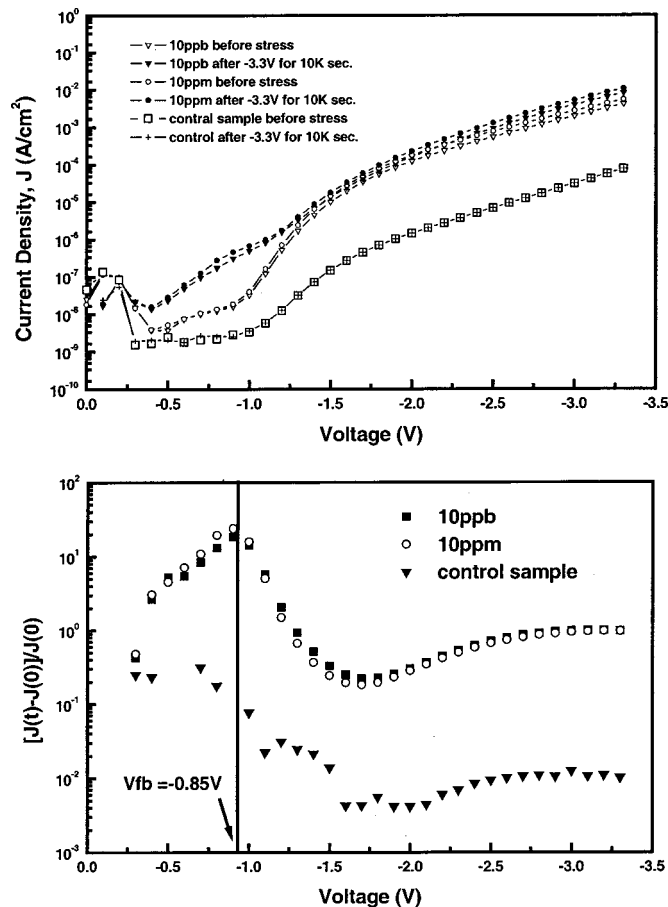


Figure 4. (a, top) J-V characteristics of 30 Å oxides with different Cu contamination levels stressed at -3.3 V for 10,000 s and (b, bottom) current change [J(t)-J(0)]/J(0) plot of (a) to enhance the stress effect.

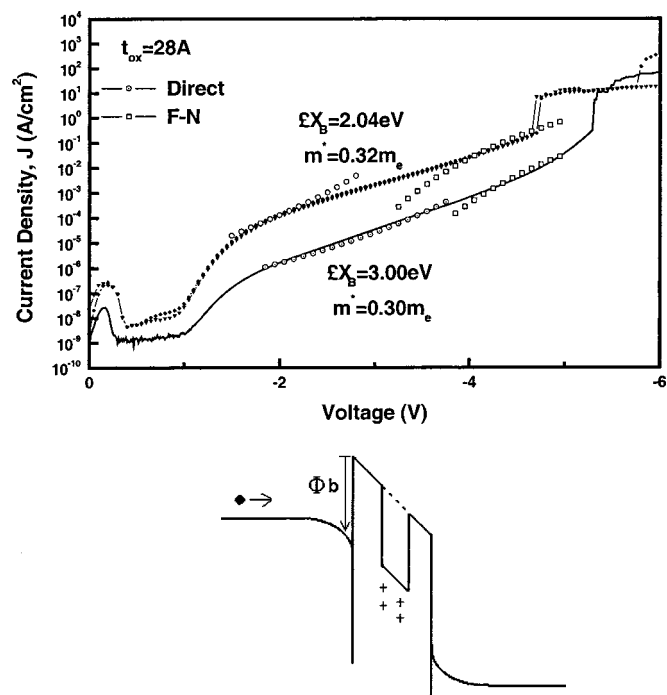


Figure 5. (a, top) Theoretically calculated and measured J-V characteristics from Fig. 1a and (b, bottom) band diagram illustrating the Cu effect in the oxide.

We have also studied the SILC effect in these samples. Figure 4a shows the stress effect on the J-V characteristics. The stress condition is -3.3 V for 10,000 s, which is equivalent to a total charge injections of 0.9 C/cm² and ~ 45 C/cm² for the control and Cu-contaminated devices, respectively. The constant voltage stress is used because it represents a more accurate stress condition for ultrathin oxide than the constant current stress. Under the same stress conditions the control oxide shows the smallest current increase. We have plotted the current change $[J(t)-J(0)]/J(0)$ to further analyze the stress effect. As shown in Fig. 4b, the current change increases with increasing Cu contamination level, and the peak values are close to the flatband voltage measured by C-V. A similar result was also reported for ultrathin oxides without contamination¹⁶ and the mechanism was attributed to be the interface trap-assisted tunneling. The reason why there is no discernible peak in the control sample is ascribed to the very small current close to the noise margin of our measurement system.

To study the cause of the large leakage current in the Cu-contaminated sample, we have analyzed the J-V characteristics using theoretical direct and F-N tunneling equations.¹⁵ Figure 5a shows the theoretically calculated and measured J-V characteristics. Good matching between the measured and calculated J-V characteristics at direct and F-N tunneling regions can be obtained in the control MOS capacitor with a barrier height of 3.0 eV and an effective mass of $0.30 m_e$. These values are close to the data published in the literature.¹³ The fitted oxide thickness of 28 Å is also close to the value measured by ellipsometry, which has an error of 6.7%. These results point out the good accuracy of the theoretical calculation. For the Cu-contaminated oxide, the best fitting result gives a barrier height and an effective mass of 2.04 eV and $0.32 m_e$, respectively. The large error between the measured and calculated currents may be due to a spread of barrier height that cannot be modeled by a single fixed barrier height value. From the theoretically calculated J-V and the measured data, it is suggested that a barrier lowering exists in the Cu-contaminated oxide. Based on this result, we propose a tunneling model in the Cu-contaminated ultrathin oxide as shown in Fig. 5b. It is known that the oxide charges or traps can

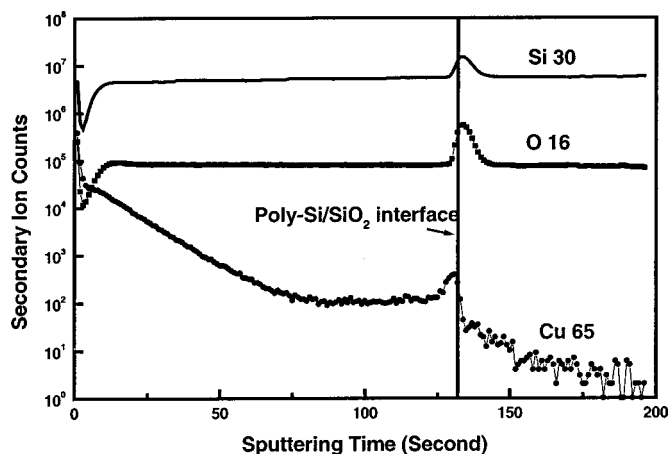


Figure 6. SIMS profile of 30 Å oxides contaminated by with ppm Cu. The Al contact was removed before SIMS analysis.

create a local energy variation inside the oxide,¹⁷ and we believe that Cu may have the same effect on the oxide. Therefore, electrons may see an effectively lower tunneling barrier as they tunnel through the oxide.

Figure 6 shows a secondary ion mass spectroscopy (SIMS) depth profile for the MOS structure. A strong Cu accumulation is observed in the poly-Si and gradually diffuses into the oxide. Although the diffusion into the oxide seems to be retarded by the amorphous structure of the oxide, Cu can still be found in the oxide. Furthermore, the presence of Cu at the Si-oxide interface can also explain the large SILC observed in Cu-contaminated samples because of the increased interface-trap density.¹² The higher number of interface-trap states can help the current tunneling as the applied voltage is less than the flatband voltage. The higher Cu concentration at the oxide-Si interface is also suggested by the C-V measurement of a thick 50 Å oxide, where the interface trap density increased from 2×10^{10} eV⁻¹/cm² in the control oxide to $\sim 2 \times 10^{11}$ eV⁻¹/cm² in the Cu-contaminated samples.

Conclusion

We have studied the gate oxide integrity of 30 Å ultrathin oxides. One to two orders of magnitude larger leakage current is observed in the pretunneling and direct tunneling region than in control devices, even at a low Cu contamination level of 10 ppb. In contrast, only the pretunneling current increase is found in thick 50 Å oxides with the same Cu level. Because of the increased leakage current, degradation of the breakdown electric field and Q_{BD} are expected. The degraded gate oxide integrity is due to the presence of Cu inside the oxide as measured by SIMS. The presence of Cu at the oxide-Si interface can also increase SILC because of the higher number of Cu-induced interface states.

Acknowledgments

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