

## Novel Strategies of FSG - CMP for Within-Wafer Uniformity Improvement and Wafer Edge Yield Enhancement Beyond 0.18 Micro Technologies

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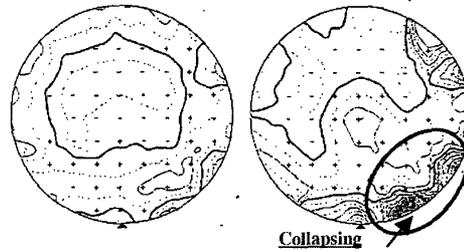
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**Abstract** - The low-K films and higher multiple stacked layers would be widely applied for ultra large-scale integrated circuits [1][2]. However, for 8" (200mm) or 12" (300mm) wafer, the phenomena of wafer edge collapsing in higher interlayer low-K dielectric film causes from CMP polishing effect. (Shown in Fig. 1). Conventionally a amount of work has been developed in the optimization of different parameters, such as low pressure and high speed [3], metal dummy filling [4], harder pad used [4], and design of polishing head in order to resolve the problems. But these methods only engaged in design of experiment, not addressed in CMP theory of edge collapsing and controlling way. In this paper we will discuss the theory applied in Preston equation to explain the polishing behavior in wafer edge. In advance, to implement the theory, we adopted novel strategies, including of different polishing head (sweep) vibration and pad edge sprayer methods, even new wafer retaining ring design and novel delivery slurry methods in advance. The characteristics of within wafer nonuniformity and edge profile against CMP polishing low-k films, fluorinated silicate glass (FSG), would be evaluated in this new strategy action. Besides, the dimension of metal line and VIA, and edge die-yield can be directly responded to the edge profile improvement. From the action results, the average 7~10% yield improvement of 0.18 technology can be achieved, especially 15% edge-die yield improvement. The edge profile could promote the phenomena of no collapsing from the original 75 mm to 95 mm of wafer center-to-edge distance, excluding 3 mm edge of 8-inch wafer. These high efficient strategies for within-wafer planarization and edge profile is also proven and fulfilled with the reducing over 50% VIA CD deviation on the rule of lithography.

**Index Terms** - Fluorinated silicate glass (FSG), chemical-mechanical planarization (CMP), uniformity, wafer edge, polishing path, head sweep profile, and edge sprayer.



**Fig.1** Edge collapsing appeared in FSG intermetal dielectric film of 0.18 technology after OX-CMP. (a) Thickness Map before OX-CMP; (b) Thickness Map after OX-CMP.

### INTRODUCTION

For a HDP CVD-FSG deposition characteristic, there is the center-to-edge thickness gradients created in the wafer (shown in Fig. 1(a)). But the following CMP processes are always required to compensate for the deposition characteristics to achieve the integration of nonuniformity of inter-metal dielectric films. From the Preston's or other simulated equation [1], the removal rate is proportional to the relative polishing velocity in wafer holder and polishing pads. The higher rotated speed of pad is, the higher removal rate is. While the dielectric film polishing in the example of a rotary CMP, the gradient of edge-to-center polishing rate exists in the polishing path. Hence, the phenomena of edge collapsing can be easily induced from CMP polishing behavior, especially enhanced with the low-K film characteristic of HDP CVD deposition. Besides, if the wafer were hold and polished in the pad edge with more portions, the wafer edge would be much seriously collapsed. To improve the integration issue of wafer edge collapsing, the reduction of edge polishing rate within a wafer can be proposed by the new developed polishing path and edge sprayer methods. The polishing path can be calculated and simulated by the Preston's

theory. Fig. 2 is shown on the relation between the relative velocity and time with original and new polishing head sweeps in a pad. The new head sweep method adopt to keep more stable relative polishing speed of wafer to pad with time increasing. Fig.3 is also demonstrated with the comparison of the original and new paths. The new developed wafer-polishing path is more close to a pad center, but the same sweep range across the pad. The concept mainly attempts to keep the wafer holding in the center of pad with more portions, in order to eliminate the polishing ratio in pad edge with the higher removal rate.

In addition, another approach is to directly reduce the removal rate in pad edge with edge sprayer to dilute slurry concentration. Because the slurry concentration is proportional to the removal rate, the edge sprayer could spread the water within 1~3 inches range around pad edge to reduce the removal rate.

These works would be evaluated and performed with VIA CD variations, edge yield promotion, with-in-wafer non-uniformity (WIWNU), and stacked film thickness profiles to adjust the optimization of these developed process parameters.

### EXPERIMENT

Experiments were carried out on an Applied Material Mirra CMP system with a multiplaten and multihead configuration. There is a sequential two-platen polisher and the following oxide buff step on the third platen. Various hardnesses of pads used in the multiplaten system, such as Rodel IC1000 and IC1010, were compared in the marathon test of 11K Å CVD-FSG blanket wafers. A diamond disk conditioner was employed in-situ to wafer polishing. The polishing path could be adjusted within the various recipes. Besides, the edge sprayer is designed with the nozzle head to spread de-ion water installed around the slurry delivery arm.

SEM measurement was used to analyze the VIA CD dimension within the wafer after VIA etch process. To demonstrate the thickness of removed dielectric film with increased time, a Nanometric 8000 XSE tool measured the stacked film thickness and profile.

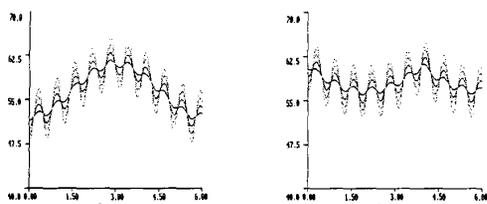


Fig.2 Relative velocity from wafer to pad with different polishing sweep methods.

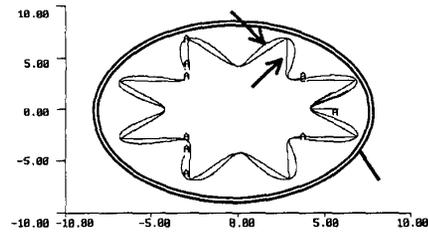


Fig.3 (a) Wafer polishing path in a pad, compared with different polishing head sweeps. It's shown on the relative motion of a wafer to the platen.

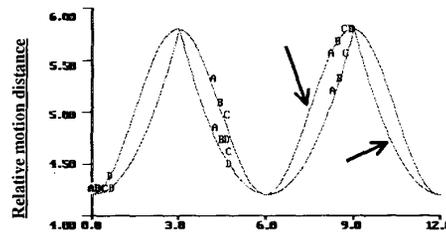


Fig.3 (b) Partial scale-up of (a) with time increase.

### Results and Discussion

#### *New developed polishing path to improve nonuniformity:*

In a rotary CMP, such as Applied Material Mirra CMP system, the original polishing path of a wafer carrier is the sinusoidal motion across the center to edge of a pad. The nonuniformity of FSG film after CMP can be kept to 5~8% with 3 mm edge exclusion (shown in Fig.1 (b)). New developed polishing path could be from the concept of the linear polishing path, which keeps the stable removal rate across a pad. From Fig.4 data of stacked FSG thickness profiles, the theory and simulation of polishing head vibration would support the experiment results and achieve below 2% uniformity, excluded 3 mm edge of FSG blanket wafers. The phenomena of edge collapsing could be made from the original sinusoidal polishing path. The higher stacked films in the multi-metal layers would make more seriously collapsing in wafer edge, because of CMP rounding the edge. Fig. 5 explains the perfect scheme of stacked films used these strategies from original to better edge profile.

#### *Edge sprayer performance:*

In addition of polishing paths to improve the nonuniformity, another strategy can adopted with edge

DIW sprayer, due to use DIW dilute the higher removal rate performed in pad edge. The deviation of post thickness from wafer center to edge would be proportioned to DIW spreading range of edge sprayer. (Shown on Fig.6). For example, without edge sprayer, the polished FSG film in the wafer edge would be collapsed of 500 Å deviation from wafer center (0 mm) to 91 mm position in radius. With 5 cm spread range of a edge sprayer, there is non-collapsing wafer edge and best WIWNU. Hence, the best wafer edge profile can be well controlled on the proper range of DIW spreading.

Of course, the average 7~10% yield can be improved with these actions, especially 15% edge-die yield. The edge profile could promote (no collapsing) from wafer center (0 mm) to ±95 mm position with 8-inch wafer, excluding 3 mm edge. These efficient strategies for within-wafer planarization and edge profile also fulfill with the reduction of over 50% VIA CD deviation on the rule of lithography.

### Conclusions

For the technology progress, the low-K dielectric film would be widely applied in intermetal dielectric layers. Due to the rouging performance of the rotary polisher, we developed the different strategies to improve the edge collapsing phenomena in the low-K film, including the novel polishing path and edge sprayer. New polishing path can keep the non-collapsing edge from wafer center to 95 mm position, excluding 3mm edge. Edge sprayer takes the advantage of the dilute slurry concept to eliminate the highest removal rate in pad edge. These integrated actions can simultaneously rescue the collapsing edge profile, even over 50% VIA CD deviation reduction and 15% edge yield improvement.

In advance, another ideas, such as new polishing heads and various slurry delivery methods, would be implemented and studied with different requirements of stacked films and film qualities. This work would mainly provide the novel and alternative strategies to resolve the problem in CMP systems.

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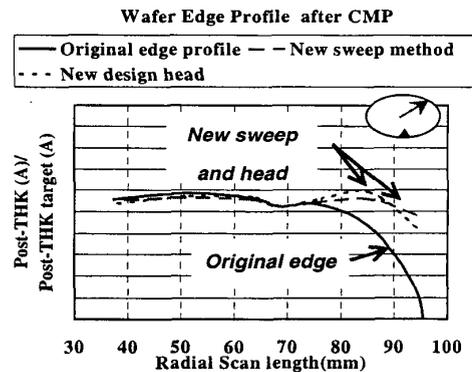


Fig. 4 Edge profile of the 5<sup>th</sup> interlayer dielectric films in product with different head sweeps (after CMP).

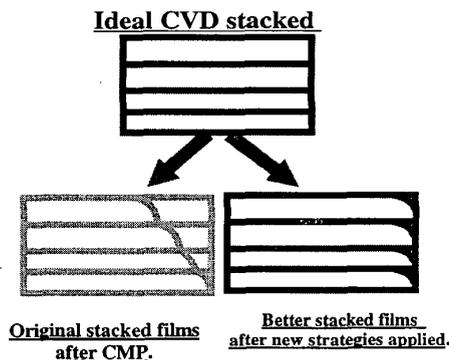


Fig. 5 Scheme of better stacked films after new strategies applied in CMP.

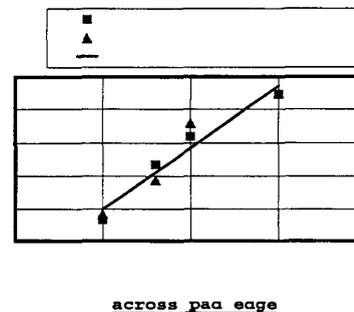


Fig. 6 Relationship between spread range of edge.

