A Comprehensive Study of Suppression of Boron Penetration by Amorphous-Si Gate in P^+-Gate PMOS Devices

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***Abstract*—This paper presents a comprehensive study of the impact of the silicon gate structure on the suppression of boron penetration in p^+-gate devices. The characteristics and reliability for different gate structures (poly-Si, α-Si, poly-Si/poly-Si, poly-Si/α-Si, α-Si/poly-Si, and α-Si/α-Si) in p^+ polygate PMOS devices are investigated in detail. The suppression of boron penetration by the nitrided gate oxide is also discussed. The comparison is based on flatband voltage shift as well as the value of charge to breakdown. Results show that the effect of boron diffusion through the thin gate oxide in p^+ polygate PMOS devices can be significantly suppressed by employing the as-deposited amorphous silicon gate. Stacked structures can also be employed to suppress boron penetration at the expense of higher polygate resistance. The single layer as-deposited amorphous silicon is a suitable silicon gate material in the p^+-gate PMOS device for future dual-gate CMOS process. In addition, by employing a long time annealing at 600°C prior to p^+-gate ion implantation and activation, further improvements in suppression of boron penetration, polygate resistance, and gate oxide reliability can be achieved for the as-deposited amorphous-Si gate. Modifying the silicon gate structure instead of the gate dielectrics is an effective approach to suppress the boron penetration effect.**

I. Introduction

P^+ polygate is essential when P-MOSFET is scaled down to the deep submicrometer regime. The surface-channel device with p^+ polygate has been investigated [1] in place of the buried-channel device with the n^+ polygate due to superior short-channel behavior, better turn-off characteristics, a lower threshold voltage operation, much less sensitive to process tolerances [2], and improved hot-carrier reliability [3]. Furthermore, the buried-channel carrier freeze-out problem in the channel region for 77 K operation can be avoided [4]. However, the penetration of boron impurity from the p^+-doped electrode through the thin gate oxide into the channel region is a critical issue [5]–[8]. Especially, boron penetration is aggravated when annealing in the presence of hydrogen [5], [9], [10] or fluorine [6], [7]. We can eliminate the effect of hydrogen on the boron penetration by avoiding the presence of hydrogen after p^+ poly doping in the annealing furnaces. However, many processes inadvertently introduce fluorine near the gate oxide such as CVD W and WSi_2 through WF_6 decomposition, fluorine-based plasma contact hole etching, and BF_2 source/drain implants. This becomes a major issue in design of the deep submicrometer PMOS device with p^+ polygate. The boron penetration effect can cause shifts of flatband voltage (V_{FB}), distortion of capacitance-voltage (C-V) curves, increase of the subthreshold swing (S) and leakage current, and deterioration of the gate oxide quality. Thus, to keep the desired performance of the surface-channel PMOS device, boron penetration should be eliminated.

Various approaches have been proposed to suppress the boron penetration effect [11]–[25]. Most of the previous stud-

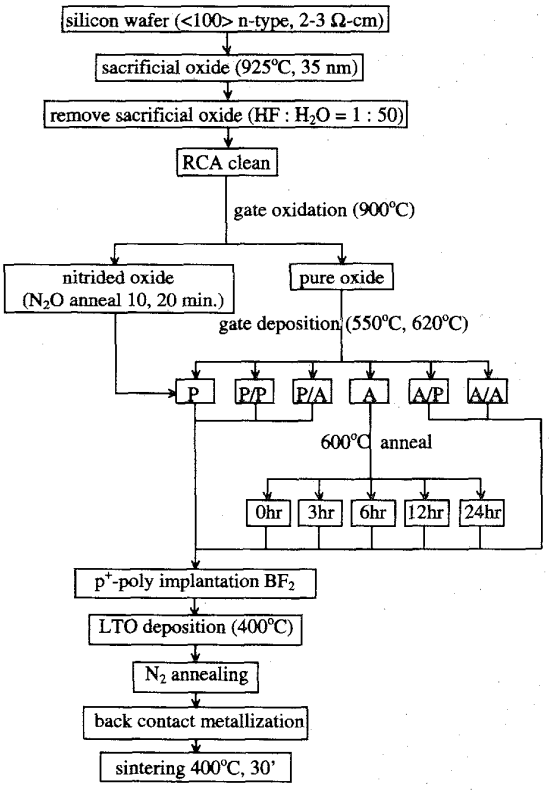

Fig. 1. Sample preparation procedure.

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TABLE I
KEY THERMAL OXIDATION PROCESSES IN N_2O-ANNEALED GATE OXIDE EXPERIMENT

	Diluted O_2 Oxidation	Pure N_2O Annealing	Pure N_2 Annealing
Pure Oxide (Control)	900°C, 66'	–	900°C, 10'
10' N_2O-Annealed Oxide	900°C, 46'	900°C, 10'	900°C, 20'
20' N_2O-Annealed Oxide	900°C, 38'	900°C, 20'	900°C, 18'

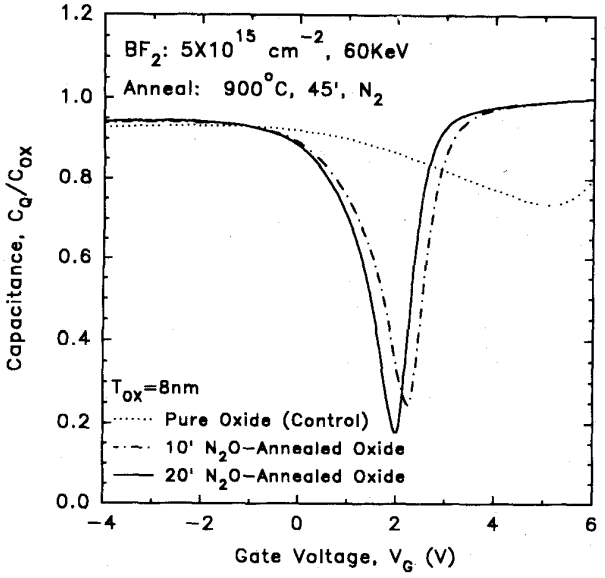


Fig. 2. The measured quasi-static C-V curves for MOS capacitors with control and N_2O annealed gate dielectrics.

ies focus on the topic in strengthening the gate dielectrics to reduce the boron penetration effect. Thermally nitrided gate oxide in NH_3 or N_2O ambient was suggested as a solution for suppressing boron penetration and the associated problems [11]–[20]. A good impurity barrier to boron penetration was achieved by such a thermally nitrided gate oxide or reoxidized nitrided oxide. Unfortunately, the nitridation process introduces a large number of electron traps [26] and a relatively high fixed oxide charge density [27], [28]. These traps and oxide charges result in threshold voltage shift, mobility degradation, and reduced stability under electrical stress. Although to reoxidize or anneal the nitrided oxide at high temperature can improve the dielectric properties by reducing the density of electron traps, such high temperature step may be problematic and undesirable for future deep submicron CMOS processes. Instead of such nitrided oxide, another approach is to modify the microstructure of silicon gate electrode to suppress the boron penetration effect, such as to form a large grain size from as-deposited amorphous silicon [21], [23], and stacked amorphous silicon films [22]. Less boron penetration effect was obtained and was attributed to suppressed fluorine and boron diffusion in the as-deposited amorphous silicon gate and/or a longer diffusion path in the stacked amorphous silicon layer. However, no comprehensive study of boron penetration in the p^+-doped silicon gate is

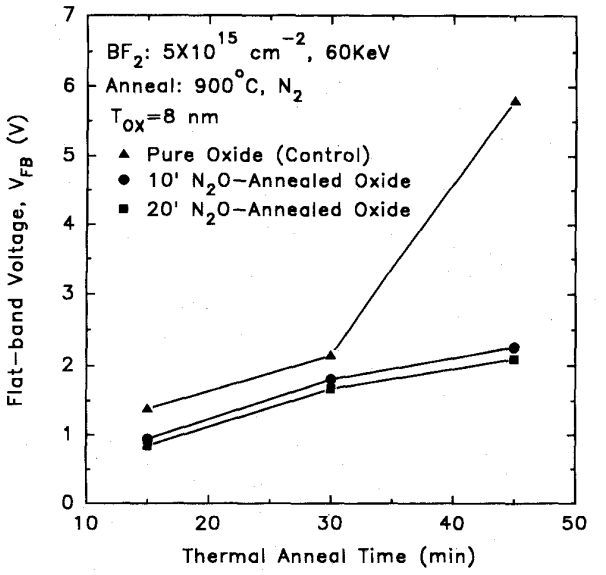


Fig. 3. Flatband voltage for MOS capacitors with different gate dielectrics as a function of post-implant anneal time.

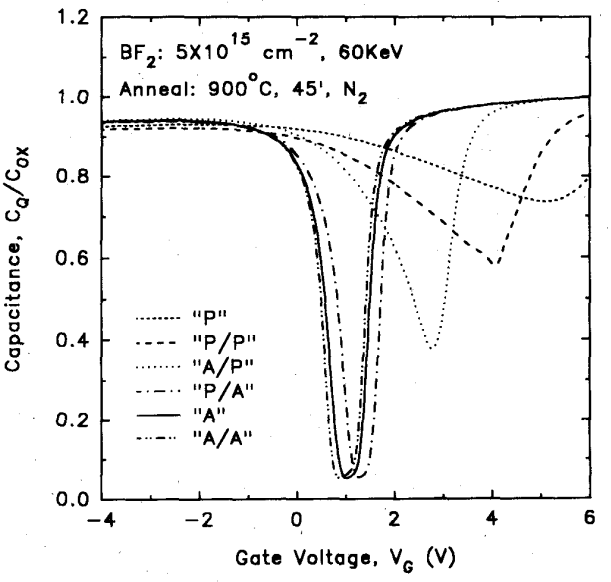


Fig. 4. The measured quasi-static C-V curves for MOS capacitors with different silicon gate structures.

available to examine what is responsible for the retardation of boron diffusion in such stacked gate structures.

In this paper we first examine the effect of nitrided oxide on the retardation of boron penetration. Boron penetration can be reduced by using such nitrided oxide. However, the results were not satisfactory. Therefore, specific changes in various silicon gate structures including single and double layer of polysilicon (poly-Si) and amorphous silicon (α-Si), and combination of poly-Si/α-Si or α-Si/poly-Si gates were attempted to examine the effect of suppression of boron penetration. In addition, an as-deposited amorphous silicon gate followed by a long time annealing at 600°C prior to the p^+-

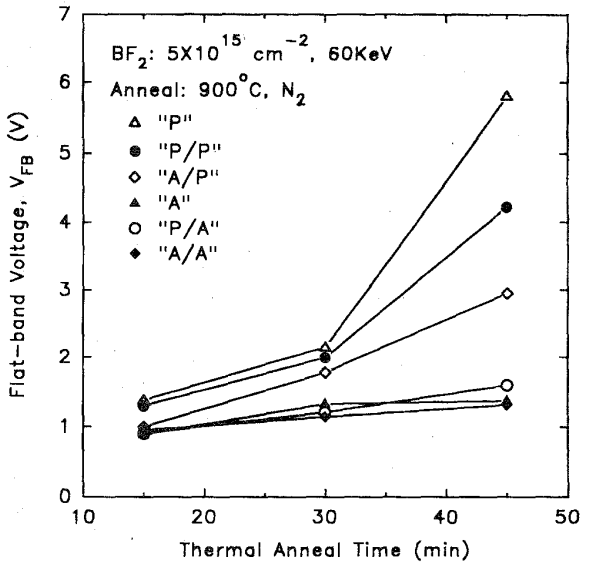


Fig. 5. Flatband voltage for MOS capacitors with different silicon gate structures as a function of post-implant anneal time.

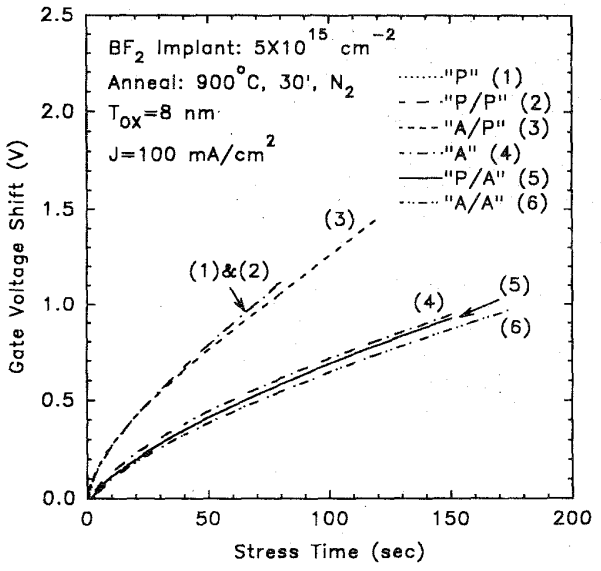


Fig. 7. Fowler-Nordheim stress under 100 mA/cm^2 positive current for p^+-gate MOS devices with various silicon gate structures.

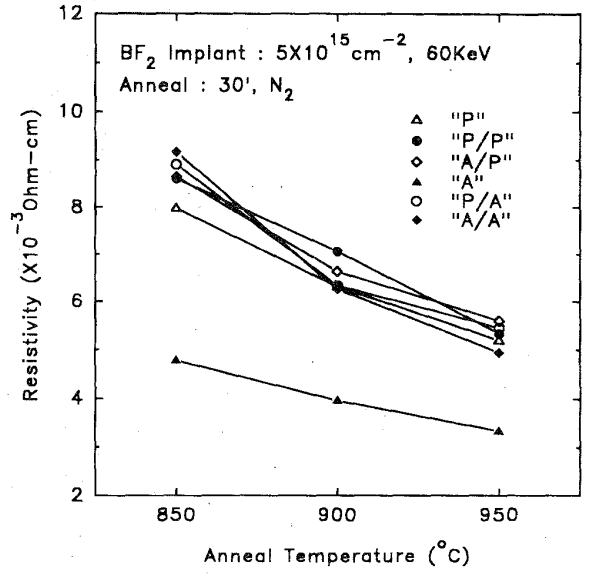


Fig. 6. Polygate resistivity for different silicon gate structures as a function of anneal temperatures.

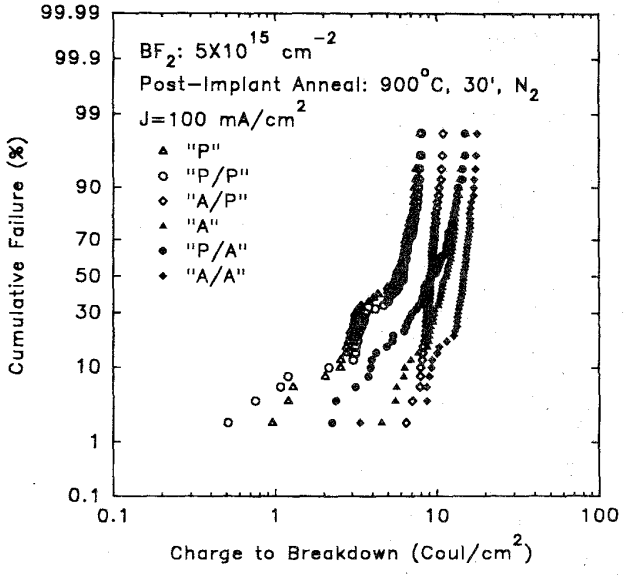
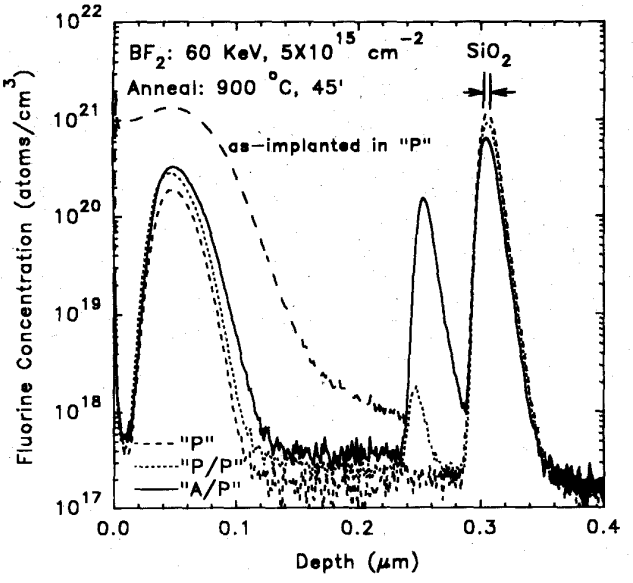


Fig. 8. Cumulative failure versus chage to beakdown for the p^+-gate capacitors with various silicon gate structures. Gate oxide thickness is 8 nm. Stress condition is 100 mA/cm^2.

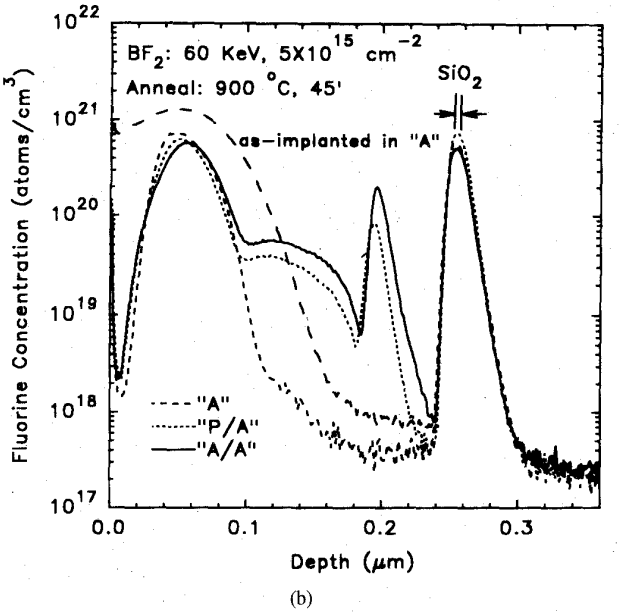
gate ion implantation and activation was employed to examine the relationship between the silicon gate microstructure and the boron penetration with fluorine incorporation.

II. Experimental Details

P^+ polygated PMOS capacitors were fabricated to evaluate the boron penetration effect. The sample preparation procedure is shown in Fig. 1. The substrates were (100)-oriented n-type silicon wafers with a resistivity of $2 \sim 3\ \Omega \cdot$ cm. To improve the gate oxide quality, the wafers were first grown a 350 Å-thick sacrificial oxide at 925°C. The sacrificial oxide was stripped and RCA-clean was performed immediately prior to growth of the gate oxide. After being cleaned, all wafers were dipped in a diluted HF solution to remove the native oxide and then loaded into the furnace. An 80 Å gate oxide was grown at 900°C in diluted O_2 ($N_2/O_2 = 6/1$). The oxide thickness was measured by NanoSpec(Nanometrics) and also verified by MOS capacitance. Undoped polysilicon with a thickness of 3000 Å was then deposited by LPCVD at 620°C immediately after the gate oxide formation. In this experiment, p^+ polygates were formed by BF_2 implantation. After the ion implantation, all wafers were coated with a low-temperature oxide (LTO) to prevent boron out-diffusion and to protect the surface of films from the ambient during the subsequent annealing cycles.

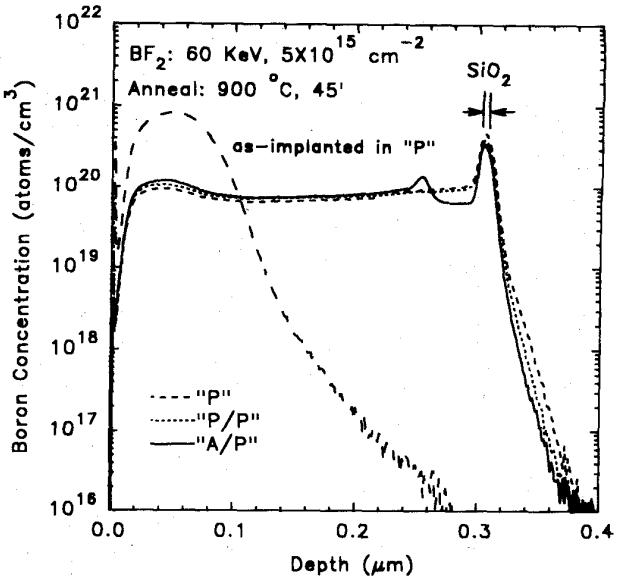


(a)

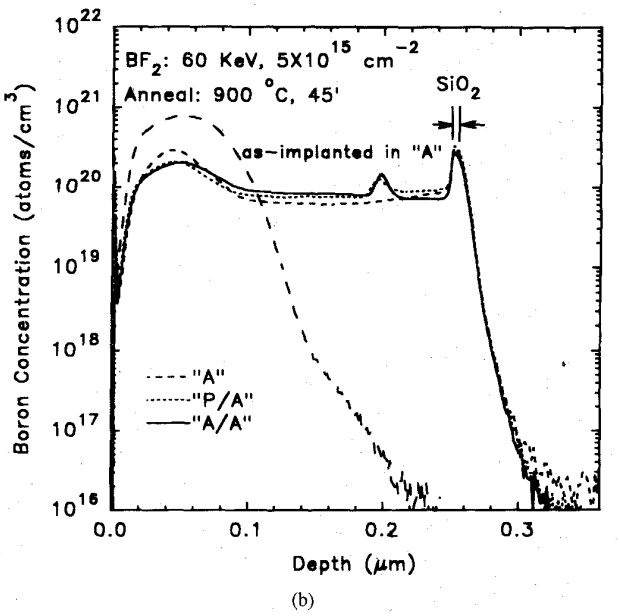


(b)

Fig. 9. Fluorine depth profiles measured by SIMS for various silicon gate structures: (a) "P," "P/P," and "A/P;" (b) "A," "P/A," and "A/A" structures. The films were implanted with BF_2 at a dosage of 5×10^{15} cm^{-2}, and then annealed at 900°C for 45 min.



(a)



(b)

Fig. 10. Boron depth profiles measured by SIMS for various silicon gate structures: (a) "P," "P/P," and "A/P;" (b) "A," "P/A," and "A/A" structures. The films were implanted with BF_2 at a dosage of 5×10^{15} cm^{-2}, and then annealed at 900°C for 45 min.

After LTO capping, the p^+-gate was annealed to investigate the boron penetration effect. All anneals were performed in a dry nitrogen ambient. Finally, pad aluminum metallization, back contact aluminum metallization, and sintering (400°C) processes were executed.

The experiments in this study were divided into three parts. Firstly, the effect of N_2O annealed gate oxide on suppression of boron penetration was investigated. Secondly, effects of the gate microstructure and interfacial dopant segregation in the p^+ polygate on boron diffusion was discussed by employing various gate structures. And finally, as-deposited amorphous silicon films were annealed at 600°C for various times prior to the p^+-gate implantation to examine the effect of grain microstructure on boron penetration.

A. N_2O-Annealed Gate-Oxides

Gate oxides were first grown at 900°C in diluted O_2 and then annealed in pure N_2O at oxidation temperatures of 10 min. and 20 min. Finally, a post-annealing in N_2 was employed at 900°C prior to wafers being loaded out. Control oxides were grown at 900°C in diluted O_2 and then annealed in N_2 for 10 min at the oxidation temperature. Since the N_2O

Fig. 11. Cross-sectional TEM pictures for various silicon gate structures: (a) "P," (b) "P/P," (c) "A/P," (d) "A," (e) "P/A, " and (f) "A/A" structures. The films were implanted with BF_2 at a dosage of 1×10^{16} cm^{-2}, and then annealed at 900°C for 30 min.

anneal results in increase in the oxide thickness, the oxidation time and post-annealing time were adjusted to keep the same thermal processes as well as the desired gate oxide thickness (80 Å) as that of the control oxide. The key thermal processes during gate oxidation in this experiment are listed in Table I.

B. Gate-Structure Experiments

The sample preparation is the same as the control sample in the N_2O-annealed experiment except the deposition process of the polygate. Following gate oxide formation, specific changes of the gate structure were performed to examine effects of the silicon gate microstructure [21], [23], and the stacked silicon gate structure [22], [25] on suppression of the boron penetration. Six different silicon gate structures were deposited, namely, poly-Si 3000 Å (abbreviated as "P"), poly-Si 500 Å/poly-Si 2500 Å ("P/P"), α-Si 500 Å/poly-Si 2500 Å ("A/P"), α-Si 2500 Å ("A"), poly-Si 500 Å/α-Si 2000 Å ("P/A"), and α-Si 500 Å/α-Si 2000 Å ("A/A") which is in

accordance with the deposition sequence. The poly-Si and α-Si films were deposited by LPCVD using SiH_4 gas at 620°C and 550°C, respectively. p^+-gates were doped by ion implantation of BF_2 at 60 KeV with various doses: 2×10^{15}, 5×10^{15}, and 1×10^{16} cm^{-2}. The p^+-gate implant condition was chosen such that the implant dosage was confined within the top-layer of the stacked structures, which includes "P/P," "A/P," "P/A," and "A/A," and to avoid damaging the interface of the stacked structure. The wafers were not loaded out and kept at low pressure during the deposition process for the stacked gate structures. All the wafers received a post-implant annealing and hence polycrystallized.

C. Grain-Size Experiments

In this experiment, amorphous silicon films were deposited by LPCVD furnace using SiH_4 gas at 550°C and then crystallized at 600°C, in N_2 ambient for 3 h, 6 h, 12 h, or 24 h, to examine the effect of silicon gate microstructure on suppression of boron penetration. Then, the p^+-gate was doped by BF_2 ion implantation at 50 KeV with a dosage of 5×10^{15} cm^{-2}.

Electrical measurements, C-V, and I-V, and material analyses, secondary ion mass spectrometry (SIMS), and transmission electron microscopy (TEM), were employed to examine the boron penetration effect for the fabricated samples. All C-V curves were measured from inversion to accumulation in order to reduce spurious effects due to inversion-layer response time [28]. The resistivity of the silicon gate films were measured by four-point-probe measurement.

III. Results and Discussion

A. Gate Dielectrics

Recently, low-temperature (900 $\sim$ 950°C) N_2O annealed gate oxide is shown to be a good barrier to boron penetration [20], [31]. A light N_2O anneal (950°C, 5 min, or 900°C, 20 min) for 60 $\sim$ 110 Å oxide is shown to be effective in blocking boron penetration. The suppression of boron penetration is attributed to nitrogen incorporation at Si/SiO_2 interface. Fig. 2 shows the quasi-static C-V curves of PMOS capacitors for the control and N_2O annealed oxides. The C-V curve for the control oxide is much distorted and shifted to more positive gate voltage as compared to the N_2O annealed oxides. Lower interface state density (D_{it}) for N_2O annealed oxides than that of the control oxide is also observed in the figure, as evidenced by the lower C_{min} value. Furthermore, the sample with N_2O anneal for 20 min exhibits less flatband voltage (V_{FB}) shift than the sample with N_2O anneal for 10 min, which resulted from a higher nitrogen concentration incorporated at the Si/SiO_2 interface. The V_{FB} shift as a function of thermal anneal time at 900°C in a N_2 ambient for the control and the N_2O annealed gate oxides is shown in Fig. 3. Obviously, boron penetration can be suppressed substantially by annealing the gate oxide in N_2O ambient. However, the suppression of boron penetration by N_2O annealed gate oxides does not achieve the hope-for results. Although we can further suppress boron penetration by applying a longer N_2O annealing time to increase the nitrogen incorporation at the Si/SiO_2 interface, the device speed and reliability may be degraded by the heavier nitrided oxide [30], [31]. Therefore, another approach in modifying the silicon gate structure is adopted to suppress boron penetration.

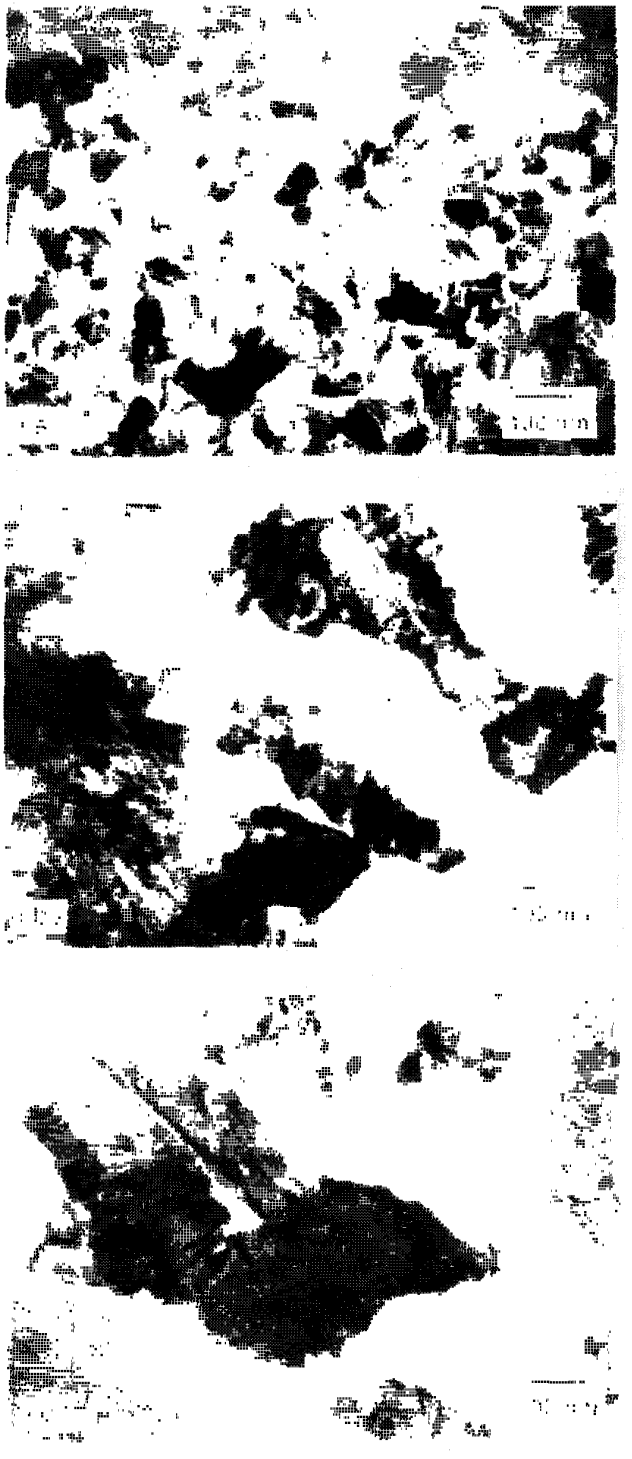


Fig. 12. TEM plan-view for various silicon gate: (a) as-deposited poly-Si gate, (b) as-deposited α-Si gate with 600°C/3 hr annealing, and (c) as-deposited α-Si gate with 600°C/24 hr annealing.

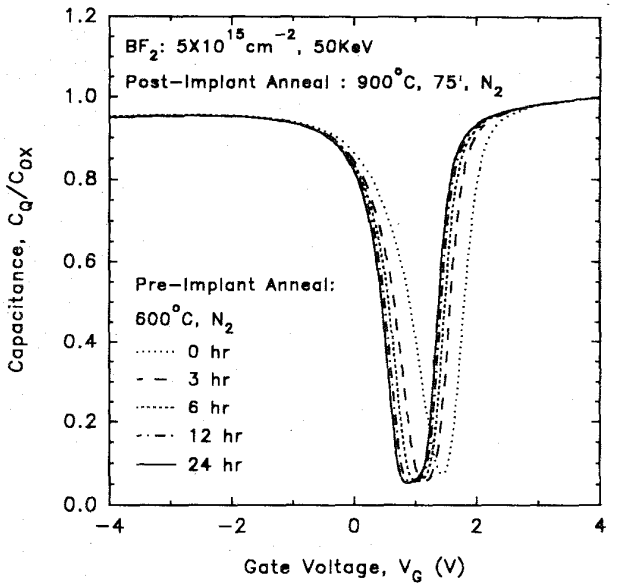


Fig. 13. The measured quasi-static C-V curves for the as-deposited α-Si gate MOS capacitors with various pre-implant anneal times.

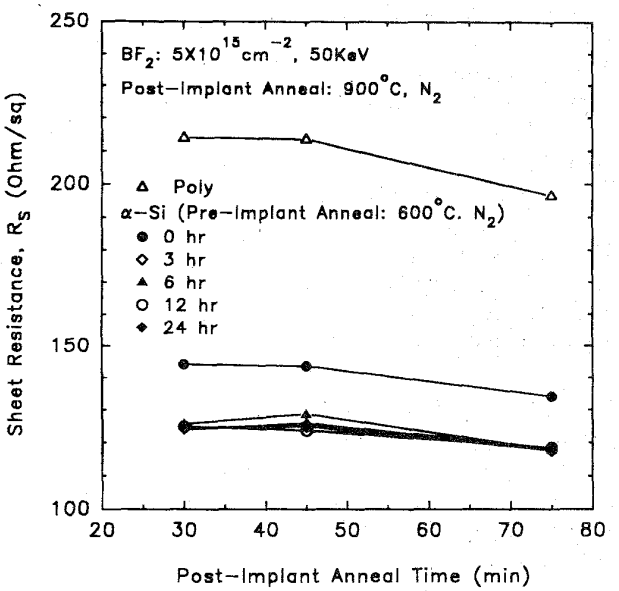


Fig. 14. Sheet resistance as a function of post-implant anneal time for the polygate formed by as-deposited poly-Si or as-deposited α-Si with various pre-implant annealing times.

B. Polysilicon Gate Structures

Various kinds of silicon gate structures are employed to examine effects of the modifying silicon gate electrode on suppression of the boron penetration. Fig. 4 shows quasistatic C-V curves for PMOS capacitors with different gate structures. Note that, for "P," "P/P," and "A/P," the C-V curves shift dramatically to the right and $C_{\min}$ shows large increases, indicating a large amount of boron penetration into the channel. The measured flatband voltages for different silicon gate structures as a function of thermal anneal time at 900°C is shown in Fig. 5. The group of "A," "P/A," and "A/A" samples demonstrate a much lower $V_{\rm FB}$ shift than the other group of "P," "P/P," and "A/P" samples, which seemingly indicates that the α-Si layer can effectively retard the boron penetration during the post-implant annealing. Furthermore, samples with stacked structure work in suppression of boron penetration, as shown in the figure. However, higher polygate resistivity are obtained for the stacked silicon gate structures as shown in Fig. 6. The "A" sample demonstrates the lowest gate resistivity among these six gate structures.

Fowler-Nordheim stressing with a constant current density of 100 mA/cm^2 was performed on PMOS capacitors to characterize the gate oxide reliability for various silicon gate structures in this experiment. Fig. 7 shows that the electron trapping efficiency in the gate oxide for the group of "A," "P/A," and "A/A" samples is lower than the other group of "P," "P/P," and "A/P" samples. The electron trapping efficiency increases with $V_{\rm FB}$ shifts as the boron penetration becomes more severe [6]. In this study, we believe that the superior gate oxide quality for "A," "P/A," and "A/A" is mainly due to less boron penetration into the Si substrate. Fig. 8 shows the cumulative failure versus charge to breakdown ($Q_{\rm bd}$) for the PMOS capacitors with various silicon gate structures. The initial failure of oxide films can be minimized by applying an as-deposited α-Si layer on the gate oxide. It has been reported that less cusps are formed at grain boundaries in the as-deposited α-Si gate due to a larger grain size [23], [32] than the as-deposited poly-Si gate. The formation of cusps will decrease the value of $Q_{\rm bd}$ and, therefore, increase the $Q_{\rm bd}$ distribution tail. Furthermore, a higher intrinsic oxide $Q_{\rm bd}$ is obtained for the group of "A," "P/A," and "A/A" samples, which exhibit less boron penetration. It is once again shown that the as-deposited α-Si layer is a promising gate material for future dual-poly gate CMOS technology development. Compared to previous results in N_2O-annealed gate oxides (Figs. 2 and 3), the as-deposited α-Si gate in p^+ polygate exhibits more resistant to boron penetration than the N_2O-annealed gate oxide does.

Fig. 9(a) and (b) shows fluorine depth profiles measured by SIMS for the group of "P," "P/P," and "A/P" samples, and the group of "A," "P/A," and "A/A" samples, respectively. It can be seen that fluorine segregates at interfaces and/or in SiO_2 due to heat-treatments [33]. Fluorine segregation at the interface of the stacked gate structure was also observed in other works [21], [22]. It resulted from the existence of an interfacial oxide layer between the top-layer and the bottom-layer. The interfacial oxide layer was formed during the deposition break due to the residual oxygen containing gas species in the LPCVD system. Since the as-deposited poly-Si exhibits a lower oxygen concentration than the as-deposited α-Si [34], the interface between the top-layer and the bottom-layer for the "P/P" sample is not as clear as the other stacked samples, as will be shown in Fig. 11. Thus, the segregation effect of fluorine and boron at the interface of the "P/P" sample is not as obvious as the other stacked samples. Since fluorine diffuses in silicon gate mainly by grain boundary diffusion [35], fluorine diffusion is more rapid in the as-deposited poly-Si film than in the as-deposited α-Si film. After annealing, the grain boundary diffusion path for fluorine

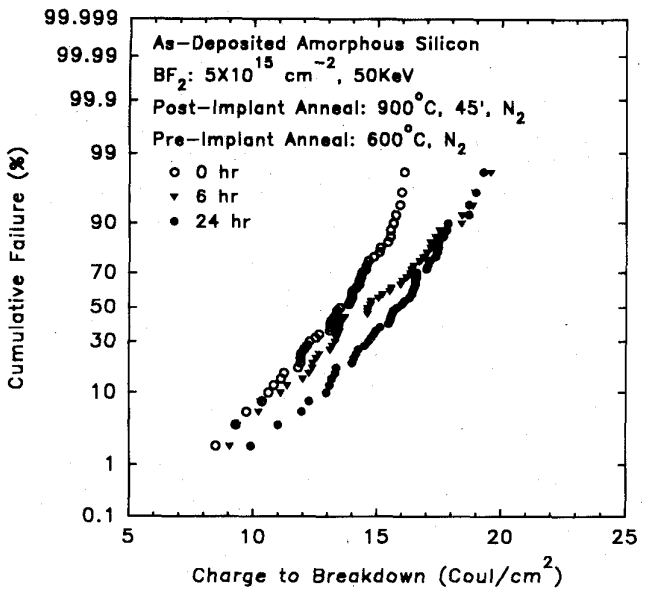


Fig. 15. Fowler-Nordheim stress under 100 mA/cm^2 positive current for the as-deposited α-Si p^+-gate MOS devices with pre-implant annealing at 600°C for 0 h, 6 h, and 24 h, respectively.

in the top-layer will be different from that in the bottom-layer. Consequently, it will result in a higher fluorine concentration at the interface of top-layer and bottom-layer for the stacked gate with an underlaid as-deposited α-Si layer than that with an underlaid as-deposited poly-Si layer, e.g., "A/P" versus "P/P," and "A/A" versus "P/A". The more fluorine is retained in the polygate electrode but not in the gate oxide, the less fluorine enhanced boron diffusion in the oxide is therefore obtained. Furthermore, the fluorine profiles for the "P/A" and "A/A" samples show a hump between the interfacial oxide layer and the fluorine peak near the gate surface. This anomalous hump was also observed in the fluorine SIMS profiles by Wu *et al.* [22]. It is suspected to result from the effect of oxygen impurities in the α-Si layer and the interfacial oxide layer [36]. The boron depth profiles for various silicon gate structures are shown in Fig. 10(a) and (b). As expected, the as-implanted profile is confined to the top-layer of the stacked structure. After the 900°C, 45 min. anneal, boron atoms diffused over the entire polygate electrode, while some segregate at the interface of the stacked structure. The pile-up of boron at the interface of the stacked layers seems to suggest less boron will penetrate into the Si substrate through the gate oxide for the stacked gates. Fig. 11 shows cross-sectional TEM pictures for various gate structures after 900°C annealing for 30 min. The texture of the stacked structures reveals that there exists a mismatched structure at the interface of top-layer and bottom-layer. As shown in the TEM micrographs, the poly-Si layer has columnar grain structure and exhibits a much smaller grain size, and consequently more grain boundaries, than the as-deposited α-Si layer. These further support the previous grain boundary diffusion mechanism for fluorine atoms.

C. Polysilicon Gate Microstructures

From the previous results, it is found that employing the as-deposited α-Si gate in p^+-gate devices suppresses the boron penetration effect and achieves low polygate resistance. Therefore, a further insight study into the effects of microstructure of the α-Si layer on suppression of boron penetration was performed. A split on annealing times for 0 hr, 3 hr, 6 hr, 12 hr, or 24 hr, at 600°C in N_2 ambient, was carried out to crystallize the as-deposited α-Si layer prior to p^+-poly implantation. The planar TEM micrographs of the as-deposited poly-Si, the as-deposited α-Si with pre-implant anneal for 3 h and 24 h are shown in Fig. 12. The as-deposited α-Si layer with a long time pre-implant annealing exhibits a much larger grain size compared to the as-deposited poly-Si layer. Fig. 13 shows the quasistatic C-V curves for as-deposited α-Si gate with different pre-implant anneal time at 600°C. Results show that the longer the pre-implant anneal time is performed, the better C-V characteristics is obtained. In addition to less V_{FB} shift, lower polygate resistance is obtained for the pre-implant annealed samples, as shown in Fig. 14. Results of Fowler-Nordheim stressing show that much better gate oxide reliability is also obtained, as shown in Fig. 15. It is suspected that improvements of the experimental results by performing a long time pre-implant annealing are due to less grain boundary diffusion path is available during the post-implant annealing.

IV. Conclusion

A systematic study of effects of the silicon gate structure and gate dielectrics on suppression of boron penetration in p^+-gate devices is presented. The boron penetration effect can be significantly suppressed by employing an as-deposited α-Si gate. In addition to suppression of boron penetration, the lowest polygate resistance can be obtained using the as-deposited α-Si gate. Stacked structure can further suppress the boron penetration. However, high gate resistance of such stacked structures is undesirable from the viewpoint of circuit speed. Furthermore, the flatband voltage shift for the as-deposited α-Si gate is very close to that of the stacked α-Si gate. Thus, the stacked structure is not necessary as long as the as-deposited α-Si gate is applied in p^+-gate PMOS devices. The resistance against the boron penetration can be further improved by employing a long time pre-implant annealing at 600°C for the as-deposited α-Si gate. Results show that microstructure of the silicon gate plays an important role in suppressing the boron penetration effect. The as-deposited α-Si gate shows good promise for future dual-gate CMOS application.

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