

Oxygen-Dependent Instability and Annealing/Passivation Effects in Amorphous In–Ga–Zn–O Thin-Film Transistors

Wei-Tsung Chen, Shih-Yi Lo, Shih-Chin Kao, Hsiao-Wen Zan, Chuang-Chuang Tsai, Jian-Hong Lin, Chun-Hsiang Fang, and Chung-Chun Lee

Abstract—This letter discusses the reason for the instability of amorphous indium–gallium–zinc–oxide (a-IGZO) thin-film transistors (TFTs) under both positive and negative bias stresses. This instability is significantly influenced by the oxygen content in the bulk IGZO and the surrounding environment. The as-fabricated low-temperature devices can only endure a single polarized bias stress. An a-IGZO TFT that is stable toward both positive and negative bias stresses with large relaxation times of 95×10^4 and 371×10^4 s, respectively, is achieved by annealing and passivation.

Index Terms—Bias stress, IGZO, stability.

I. INTRODUCTION

AMORPHOUS metal–oxide thin-film transistors (TFTs) such as amorphous indium–gallium–zinc–oxide (a-IGZO) TFTs have excellent field-effect mobility, rendering them potential candidates for replacing the conventional Si-based TFTs [1], [2]. However, a common problem faced by IGZO transistors is the instability of the threshold voltage (V_{th}) during device operation. Many studies have investigated the influences of the dielectric [3], pressure [4], temperature [5], stress mode (constant or pulsed bias) [6], [7], and passivation [8]. However, most of these studies focused on single polar gate-to-source (V_G) bias stresses; the stability at various fabrication stages has not yet been sufficiently investigated. In this letter, both positive and negative gate-to-source bias stresses were applied to fully assess the stability of the a-IGZO TFT. The stability was found to be strongly dependent on the oxygen content in both the bulk IGZO and the surrounding environment. The as-fabricated devices could only endure a single polar bias stress. The results revealed the intrinsic problem of a-IGZO TFTs fabricated at low temperatures. The conventional posttreatments, thermal annealing, and

passivation are also affected by the oxygen content. A stable TFT device that can endure both positive and negative bias stresses can be fabricated by using both thermal annealing and passivation. In this letter, a-IGZO TFTs were fabricated by a method consisting of many phases.

II. EXPERIMENTAL PROCEDURE

A 100-nm-thick silicon nitride (SiN_x) layer was used as the dielectric. The layer was deposited on a heavily doped silicon wafer by low-pressure chemical vapor deposition at 780 °C with NH_3 and SiH_2Cl_2 reactant gases. A 35-nm-thick layer of a-IGZO (In:Ga:Zn = 1:1:1) was deposited on SiN_x by radio-frequency (RF) sputtering through a shadow mask. The RF power and pressure were 100 W and 3 mtorr, respectively. A mixture of oxygen and argon was introduced during sputtering. The ratio of oxygen to the mixture gas (oxygen ratio) was varied from 0% to 0.31%. A bottom-gate top-contact a-IGZO TFT (as-fabricated device; phase 1) was obtained by depositing a 50-nm-thick layer of aluminum through a shadow mask to form the source and drain contacts. The resultant device was annealed at 400 °C in a nitrogen furnace for 1 h to produce the annealed device (phase 2). Finally, a passivation layer of an organic photoresistor (1 μm) was deposited on select devices. The devices were then annealed at 200 °C for 1 h to form passivated devices (phase 3). The device channel length (L) and width (W) were fixed at 400 and 1000 μm , respectively.

III. RESULTS AND DISCUSSION

Fig. 1(a) shows the transfer characteristics of the as-fabricated devices (phase 1; fully low-temperature-fabricated devices) fabricated at various oxygen ratios ranging from 0% to 0.31%. The oxygen content in the a-IGZO active layer strongly influences the conductivity of the IGZO film [9]. Fig. 1(b) shows the transfer characteristics of the annealed devices (phase 2) as they correspond to the oxygen ratios in phase 1. This figure shows that, after postannealing, the oxygen content and, thus, the electronic characteristics of all the devices became uniform. Moreover, there was no noticeable hysteresis on the annealed devices. Fig. 1(c) shows the transfer characteristics of the passivated devices (phase 3) as they correspond to the oxygen ratios used in phase 1. The passivation layer capped on the a-IGZO TFTs did not noticeably influence the initial electronic characteristics, which indicates that the oxygen content in IGZO remained constant. Thus, an organic photoresistor is a mild and suitable material for process-sensitive IGZO.

Manuscript received February 16, 2011; revised July 25, 2011; accepted August 13, 2011. Date of publication September 25, 2011; date of current version October 26, 2011. This work was supported by the National Science Council under Grants NSC 99-2628-E-009-010 and 97-2221-E-009-036-MY3. The review of this letter was arranged by Editor A. Nathan.

W.-T. Chen, S.-Y. Lo, S.-C. Kao, H.-W. Zan, and C.-C. Tsai are with the Department of Photonics, the Institute of Electro-Optical Engineering, and the Display Institute, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: WeiChungChen@itri.org.tw; nickwork.tw@gmail.com; light.eo92g@nctu.edu.tw; hsiaowen@mail.nctu.edu.tw; ctsai7@mail.nctu.edu.tw).

J.-H. Lin, C.-H. Fang, and C.-C. Lee are with the AU Optronics Corporation, Hsinchu 300, Taiwan (e-mail: Jian.Hong.Lin@auo.com; Kevin.CH.Fang@auo.com; Yama.CC.Lee@auo.com).

Color versions of one or more of the figures in this letter are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/LED.2011.2165694

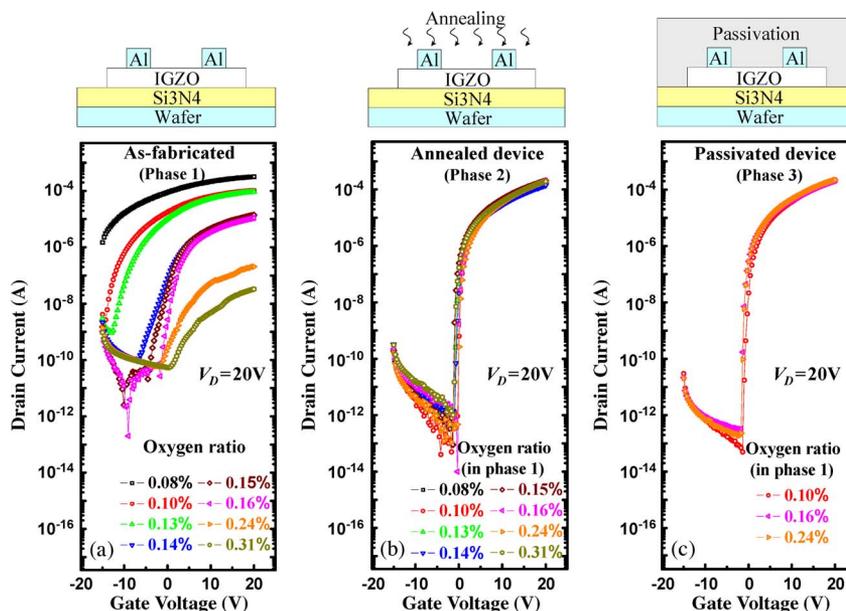


Fig. 1. Transfer characteristics of (a) as-fabricated, (b) annealed, and (c) passivated devices fabricated under various oxygen ratios during active layer deposition.

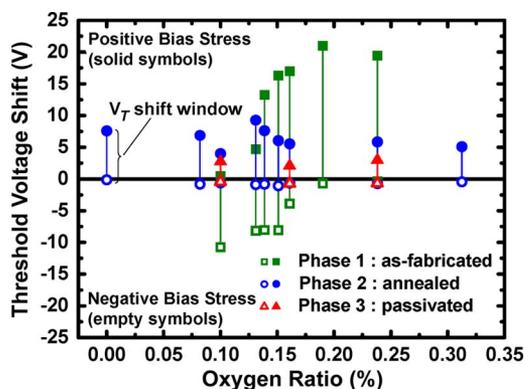


Fig. 2. Threshold voltage shifts after examinations of both positive and negative bias stresses, with each stress applied for 5000 s, plotted as a function of the oxygen ratio used during IGZO layer deposition. The devices in three fabrication phases were compared: as-fabricated, annealed, and passivated devices.

Only a few papers have discussed negative and positive gate-to-source bias stresses concurrently [7], and the relationship between the TFT instabilities under positive and negative bias stresses is not clear. Fig. 2 shows the threshold voltage shifts that occur after the stresses of both polarities were developed in the devices during the various fabrication phases with varying oxygen ratios in phase 1. The positive bias stress ($V_{GS} - V_{T0} = 20$ V; $V_{DS} = 0$ V) and negative bias stress ($V_{GS} - V_{T0} = -20$ V; $V_{DS} = 0$ V) were executed over a duration of 5000 s; V_{T0} denotes V_{th} before the bias stress was developed. The stability of the as-fabricated devices under the bias stresses of both polarities was found to be poor; the V_T shift window—defined as the distance between the V_{th} shifts after negative and positive bias stresses—was always large. Thus, an oxygen-rich device is stable only against negative stress, and an oxygen-deficient device is stable only against positive stress. IGZO TFTs usually exhibit great instability under illumination-accompanied negative gate bias stress (NBLs) [10]; however, in our study, the “oxygen-rich” devices still endure NBLs well. The improved stability against negative bias stress also implies

that the hole trapping in the dielectric layer is not observed; the heavy effective mass of holes may be the reason. The stabilities of the annealed devices under both stresses were similar, because after postannealing, the oxygen content in the a-IGZO films became uniform. Moreover, the V_T shift window became narrow after annealing. After the annealed devices were subjected to passivation, they maintained good stability under negative bias stress and exhibited enhanced stability under positive bias stress.

Both interfaces of the IGZO active layer (the dielectric surface and the top surface) are capable of trapping carriers that result in the shift in V_{th} . Both types of carriers (electrons and holes) can be trapped at the interfaces during the V_G stress; each results in a different polar V_{th} shift. Electron trapping at the top air-facing surface by absorbed oxygen (O_2^-) [4], [8] leads to a positive shift in V_{th} . Passivation is generally employed to reduce this effect [8]. However, in this study, passivation alone could not stabilize the device when the samples were not subjected to thermal annealing because it can only suppress electron trapping from air. Therefore, trapped carriers at the dielectric surface were other factors that influenced the stability of the IGZO TFTs. The electron- and hole-trapping mechanisms act in opposition, according to the results shown in Fig. 2. Furthermore, the efficacy of these two trapping mechanisms strongly depends on the oxygen content in the IGZO bulk. For phase-1 devices, the occupied electron-trapping states [11] (acceptor-like) were formed more easily when the oxygen content was high, and the unoccupied hole-trapping states [10] (donorlike) were formed more easily when the oxygen content was low. Fig. 3(a) shows the energy band diagram of an IGZO TFT under a positive gate bias. The accumulated electrons near the dielectric interface were trapped by shallow acceptor-like trap states that were oxygen-related defect states. According to the previous report discussing ZnO [12], when the Fermi level is raised from valance band to conduction band, the defect formation energies of oxygen vacancy (Vo^{2+}) and oxygen ion (O^{2-}) are varied from -0.5 to 4 eV and from 8.5 to 4 eV, respectively. Note also that air is another oxygen source that

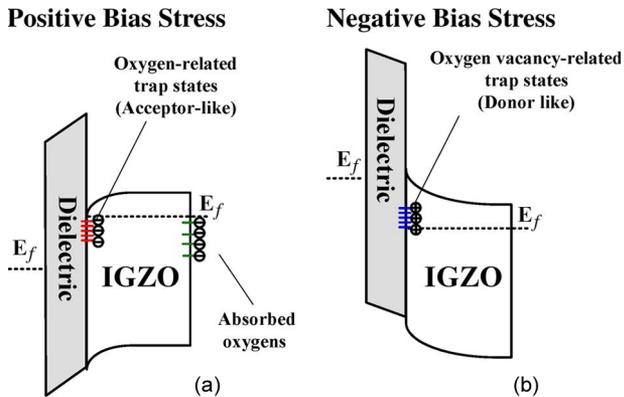


Fig. 3. Energy band diagrams under (a) positive and (b) negative bias stresses.

can trap electrons from the back channel. Fig. 3(b) shows another band diagram under a negative gate bias. The IGZO body was depleted, and the holes near the dielectric interface were trapped by deep donorlike trap states, which were oxygen-vacancy-related defect states. Moisture is also a factor that degrades the performance of the IGZO TFT by producing a leakage current [13]. This effect was not observed in this study because degradations were not apparent in phases 2 and 3.

The trap states may have resulted from the loosely bound oxygen that could move in the IGZO layer when applying the electric field. During bias stress, oxygen ions (O^{2-} ; electron-trapping state) or oxygen vacancies (V_O^{2+} ; hole-trapping state) may have been collected at the dielectric surface, resulting in the positive and negative V_{th} shifts, respectively. Chen *et al.* studied IGZO-based memory by assuming the mobility of an oxide ion (O^{2-}) in an electric field [14]. However, the actual mechanism behind the formation of the trap states is still not clear and requires further investigation.

After annealing, the overall improvement in the stability may have been a result of strengthened atomic bonding (reduction in the loosely bound oxygen content). However, the devices still did not exhibit adequate stability and exhibited “oxygen-rich” behavior, which is due to the oxygen absorbed from air.

In this letter, the stable behavior of a-IGZO TFTs under both positive ($V_{GS} - V_{T0} = 20$ V; $V_{DS} = 0$ V) and negative ($V_{GS} - V_{T0} = -20$ V; $V_{DS} = 0$ V) stresses was demonstrated. The as-fabricated devices were subjected to postannealing and passivation before attaining the final state. The extracted parameters were as follows: a mobility of 9.8 cm²/V·s, a subthreshold swing (SS) of 0.38 dec/V, a threshold voltage of 1.7 V, and an on/off ratio of 7×10^8 . The total stress duration was 10010 s. The evolution of the threshold voltage shift during stress was fitted to the stretched-exponential relaxation equation $\Delta V_T(t) = V_0[1 - \exp(-(t/\tau)^\beta)]$, where ΔV_T denotes the threshold voltage shift caused by the bias stress, τ is the characteristic time constant (relaxation time), β is the dispersion parameter, and $V_0 = V_{GS} - V_{T0}$. The τ values extracted under the positive and negative bias stresses were 95×10^4 s ($\beta = 0.35$) and 371×10^4 s ($\beta = 0.53$), respectively, which were comparable to the data reported previously for a positive bias stress [15]. Moreover, during both positive and negative gate bias stresses, the field-effect mobility and SS were maintained. The unchanged SS indicates that the electron trap states are tail states and only generated or occupied at a high gate voltage.

IV. CONCLUSION

This letter has discussed the reason for the unstable behavior of a-IGZO TFTs. Oxygen is a critical element that determines device stability under different polar bias stresses. In addition, oxygen is not only located within the bulk IGZO but also in the surrounding environment. For low-temperature devices, the V_T shift window is always large. A complete examination must involve both positive and negative bias stresses. Finally, an a-IGZO TFT that was stable under both positive and negative bias stresses was obtained. This study may open new research directions for the development of an efficient metal–oxide device with high stability.

REFERENCES

- [1] B. H. Kim, C. W. Byuna, S. M. Yoon, S. H. Yang, S. W. Jung, M. K. Ryu, S. H. K. Park, C. S. Hwang, K. I. Cho, O. S. Kwon, E. S. Park, H. C. Oh, K. H. Kim, and K. C. Park, “Oxide-thin-film-transistor-based ferroelectric memory array,” *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 324–326, Mar. 2011.
- [2] J. Y. Kwon, K. S. Son, J. S. Jung, T. S. Kim, M. K. Ryu, K. B. Park, B. W. Yoo, J. W. Kim, Y. G. Lee, K. C. Park, S. Y. Lee, and J. M. Kim, “Bottom-gate gallium indium zinc oxide thin-film transistor array for high-resolution AMOLED display,” *IEEE Electron Device Lett.*, vol. 29, no. 12, pp. 1309–1311, Dec. 2008.
- [3] L. Yuan, X. Zou, G. Fang, J. Wan, H. Zhou, and X. Zhao, “High-performance amorphous indium gallium zinc oxide thin-film transistors with HfO_xNy/HfO₂/HfO_xNy tristack gate dielectrics,” *IEEE Electron Device Lett.*, vol. 32, no. 1, pp. 42–44, Jan. 2011.
- [4] D. Kang, H. Lim, C. Kim, I. Song, J. Park, and Y. Park, “Amorphous gallium indium zinc oxide thin film transistors: Sensitive to oxygen molecules,” *Appl. Phys. Lett.*, vol. 90, no. 19, p. 192101, May 2007.
- [5] K. Hoshino and J. F. Wager, “Operating temperature trends in amorphous In–Ga–Zn–O thin-film transistors,” *IEEE Electron Device Lett.*, vol. 31, no. 8, pp. 818–820, Aug. 2010.
- [6] S. Lee, K. Jeon, J. H. Park, S. Kim, D. Kong, D. M. Kim, D. H. Kim, S. Kim, S. Kim, J. Hur, J. C. Park, I. Song, C. J. Kim, Y. Park, and U. I. Jung, “Electrical stress-induced instability of amorphous indium–gallium–zinc oxide thin-film transistors under bipolar ac stress,” *Appl. Phys. Lett.*, vol. 95, no. 13, p. 132101, Sep. 2009.
- [7] A. Suresh and J. F. Muth, “Bias stress stability of indium gallium zinc oxide channel based transparent thin film transistors,” *Appl. Phys. Lett.*, vol. 92, no. 3, p. 033502, Jan. 2008.
- [8] J. K. Jeong, H. W. Yang, J. H. Jeong, Y. G. Mo, and H. D. Kim, “Origin of threshold voltage instability in indium–gallium–zinc oxide thin film transistors,” *Appl. Phys. Lett.*, vol. 93, no. 12, p. 123508, Sep. 2008.
- [9] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, “Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors,” *Nature*, vol. 432, pp. 488–492, Nov. 2004.
- [10] K. Ghaffarzadeh, A. Nathan, J. Robertson, S. Kim, S. Jeon, C. Kim, U. I. Chung, and J. H. Lee, “Instability in threshold voltage and subthreshold behavior in Hf–In–Zn–O thin film transistors induced by bias- and light-stress,” *Appl. Phys. Lett.*, vol. 97, no. 11, p. 113504, Sep. 2010.
- [11] K. Nomura, T. Kamiya, M. Hirano, and H. Hosono, “Origins of threshold voltage shifts in room-temperature and annealed a-In–Ga–Zn–O thin-film transistors,” *Appl. Phys. Lett.*, vol. 95, no. 1, p. 013502, Jul. 2009.
- [12] A. Janotti and C. G. Van de Walle, “Native point defects in ZnO,” *Phys. Rev. B, Condens. Matter*, vol. 76, no. 16, p. 165202, Oct. 2007.
- [13] J. S. Park, J. K. Jeong, H. J. Chung, Y. G. Mo, and H. D. Kim, “Electronic transport properties of amorphous indium–gallium–zinc oxide semiconductor upon exposure to water,” *Appl. Phys. Lett.*, vol. 92, no. 7, p. 072104, Feb. 2008.
- [14] M. C. Chen, T. C. Chang, S. Y. Huang, S. C. Chen, C. W. Hu, C. T. Tsai, and S. M. Sze, “Bipolar resistive switching characteristics of transparent indium gallium zinc oxide resistive random access memory,” *Electrochem. Solid-State Lett.*, vol. 13, no. 6, pp. H191–H193, 2010.
- [15] M. E. Lopes, H. L. Gomes, M. C. R. Medeiros, P. Barquinha, L. Pereira, E. Fortunato, R. Martins, and I. Ferreira, “Gate-bias stress in amorphous oxide semiconductors thin-film transistors,” *Appl. Phys. Lett.*, vol. 95, no. 6, p. 063502, Aug. 2009.